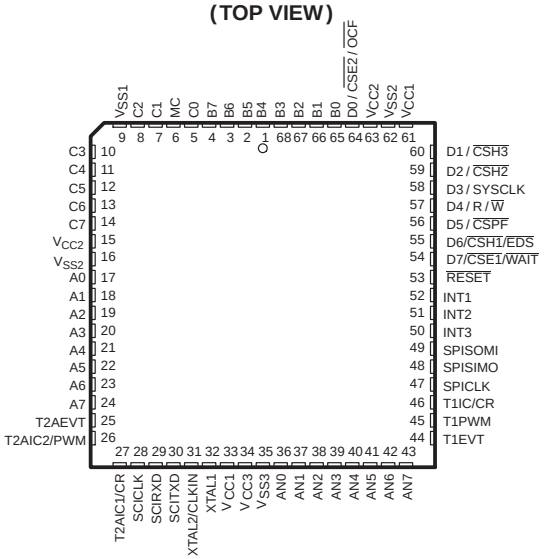
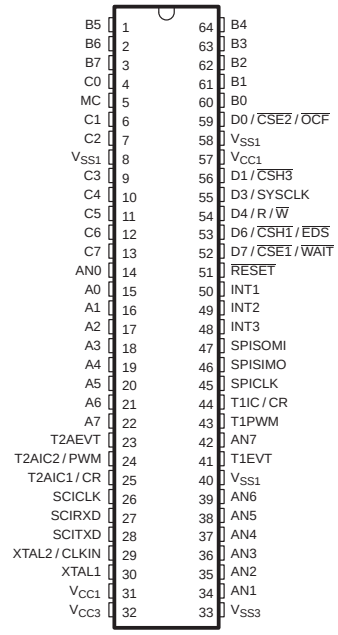
- **CMOS/EEPROM/EPROM Technologies on a Single Device**
  - **Mask-ROM Devices for High-Volume Production**
  - **One-Time-Programmable (OTP) EPROM Devices for Low-Volume Production**
  - **Reprogrammable EPROM Devices for Prototyping Purposes**
- **Internal System Memory Configurations**
  - **On-Chip Program Memory Versions**
    - **ROM: 4K to 48K Bytes**
    - **EPROM: 16K to 48K Bytes**
    - **ROM-less**
  - **Data EEPROM: 256 or 512 Bytes**
  - **Static RAM: 256 to 3.5K Bytes**
  - **External Memory/Peripheral Wait States**
  - **Precoded External Chip-Select Outputs in Microcomputer Mode**
- **Flexible Operating Features**
  - **Low-Power Modes: STANDBY and HALT**
  - **Commercial, Industrial, and Automotive Temperature Ranges**
  - **Clock Options**
    - **Divide-by-4 (0.5 MHz – 5 MHz SYSCLK)**
    - **Divide-by-1 (2 MHz – 5 MHz SYSCLK) Phase-Locked Loop (PLL)**
  - **Supply Voltage (V_{CC}): 5 V $\pm$ 10%**
- **Eight-Channel 8-Bit Analog-to-Digital Converter 1 (ADC1)**
- **Two 16-Bit General-Purpose Timers**
- **On-Chip 24-Bit Watchdog Timer**
- **Two Communication Modules**
  - **Serial Communications Interface 1 (SCI1)**
  - **Serial Peripheral Interface (SPI)**
- **Flexible Interrupt Handling**
- **TMS370 Series Compatibility**
- **CMOS/Package/TTL-Compatible I/O Pins**
  - **64-Pin Plastic and Ceramic Shrink Dual-In-Line Packages/44 Bidirectional, 9 Input Pins**
  - **68-Pin Plastic and Ceramic Leaded Chip Carrier Packages/46 Bidirectional, 9 Input Pins**
  - **All Peripheral Function Pins Are Software Configurable for Digital I/O**

FN/FZ PACKAGE
(TOP VIEW)



JN/NM PACKAGE
(TOP VIEW)



- **Workstation/PC-Based Development System**
  - **C Compiler and C Source Debugger**
  - **Real-Time In-Circuit Emulation**
  - **Extensive Breakpoint/Trace Capability**
  - **Software Performance Analysis**
  - **Multi-Window User Interface**
  - **Microcontroller Programmer**

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Pin Descriptions

PIN				I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION	SDIP (64)	LCC (68)		
A0 A1 A2 A3 A4 A5 A6 A7	DATA0 DATA1 DATA2 DATA3 DATA4 DATA5 DATA6 DATA7	15 16 17 18 19 20 21 22	17 18 19 20 21 22 23 24	I/O	Single-chip mode: Port A is a general-purpose bidirectional I/O port. Expansion mode: Port A can be individually programmed as the external bidirectional data bus (DATA0 – DATA7).
B0 B1 B2 B3 B4 B5 B6 B7	ADDR0 ADDR1 ADDR2 ADDR3 ADDR4 ADDR5 ADDR6 ADDR7	60 61 62 63 64 1 2 3	65 66 67 68 1 2 3 4	I/O	Single-chip mode: Port B is a general-purpose bidirectional I/O port. Expansion mode: Port B can be individually programmed as the low-order address output bus (ADDR0 – ADDR7).
C0 C1 C2 C3 C4 C5 C6 C7	ADDR8 ADDR9 ADDR10 ADDR11 ADDR12 ADDR13 ADDR14 ADDR15	4 6 7 9 10 11 12 13	5 7 8 10 11 12 13 14	I/O	Single-chip mode: Port C is a general-purpose bidirectional I/O port. Expansion mode: Port C can be individually programmed as the high-order address output bus (ADDR8 – ADDR15).
INT1 INT2 INT3	NMI — —	50 49 48	52 51 50	I I/O I/O	External (nonmaskable or maskable) interrupt/general-purpose input pin External maskable interrupt input/general-purpose bidirectional pin External maskable interrupt input/general-purpose bidirectional pin
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	E0 E1 E2 E3 E4 E5 E6 E7	14 34 35 36 37 38 39 42	36 37 38 39 40 41 42 43	I	ADC1 analog input (AN0 – AN7) or positive reference pins (AN1 – AN7) Port E can be individually programmed as general-purpose input pins if not used as ADC1 analog input or positive reference input.
V_{CC3} V_{SS3}		32 33	34 35		ADC1 positive-supply voltage and optional positive-reference input pin ADC1 ground reference pin
$\overline{RESET}$		51	53	I/O	System reset bidirectional pin. $\overline{RESET}$, as an input, initializes the microcontroller; as open-drain output, $\overline{RESET}$ indicates an internal failure was detected by the watchdog or oscillator fault circuit.
MC		5	6	I	Mode control (MC) pin. MC enables EEPROM write-protection override (WPO) mode, also EPROM V_{PP}.
XTAL2/CLKIN XTAL1		29 30	31 32	I O	Internal oscillator crystal input/external clock source input Internal oscillator output for crystal
V_{CC1}		31, 57	33, 61		Positive supply voltage
V_{CC2}		—	15,63		Positive supply voltage

† I = input, O = output
‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Also, port D3 can be configured as SYSCLK.

Pin Descriptions (Continued)

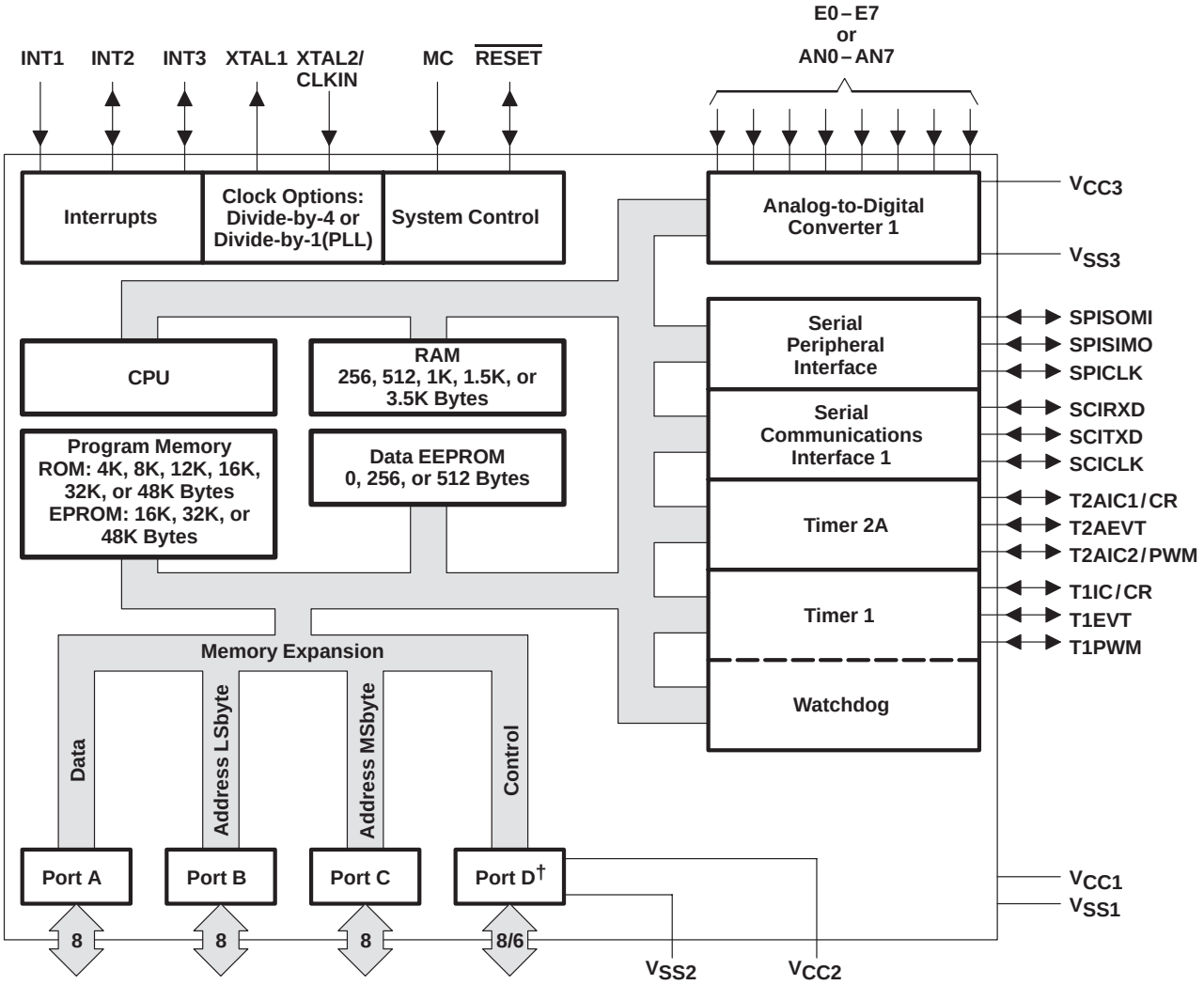
PIN					I/O†	DESCRIPTION‡
NAME	ALTERNATE FUNCTION		SDIP (64)	LCC (68)		
V_{SS1}			8, 58,40	9		Ground reference for digital logic
V_{SS2}			—	16,62		Ground reference for digital I/O logic
	FUNCTION				I/O	Single-chip mode: Port D is a general-purpose bidirectional I/O port. Each of the port D pins can be individually configured as a general-purpose I/O pin, primary memory control signal (function A), or secondary memory control signal (function B). All chip selects are independent and can be used for memory bank switching. Refer to Table 1 for function A memory accesses.
	A	B				
D0	$\overline{CSE2}$	$\overline{OCF}$	59	64		I/O pin A: Chip select eighth output 2 goes low during memory accesses I/O pin B: Opcode fetch goes low during the opcode fetch memory cycle.
D1	$\overline{CSH3}$	—	56	60		I/O pin A: Chip select half output 3 goes low during memory accesses. I/O pin B: Reserved
D2	$\overline{CSH2}$	—	—	59		I/O pin A: Chip select half output 2 goes low during memory accesses. I/O pin B: Reserved
D3	SYSCLK	SYSCLK	55	58		I/O pin A, B: Internal clock signal is 1/1 (PLL) or 1/4 XTAL2/CLKIN frequency.
D4	R/$\overline{W}$	R/$\overline{W}$	54	57		I/O pin A, B: Read/write output pin
D5	$\overline{CSPF}$	—	—	56		I/O pin A: Chip select peripheral output for peripheral file goes low during memory accesses. I/O pin B: Reserved
D6	$\overline{CSH1}$	$\overline{EDS}$	53	55		I/O pin A: Chip select half output 1 goes low during memory accesses. I/O pin B: External data strobe output goes low during memory accesses from external memory and has the same timings as the five chip selects.
D7	$\overline{CSE1}$	$\overline{WAIT}$	52	54		I/O pin A: Chip select eighth output goes low during memory accesses. I/O pin B: Wait input pin extends bus signals.
SCITXD SCIRXD SCICLK	SCIIO1 SCIIO2 SCIIO3		28 27 26	30 29 28	I/O	SCI transmit data output pin/general-purpose bidirectional pin (see Note 1) SCI receive data input pin/general-purpose bidirectional pin SCI bidirectional serial clock pin/general-purpose bidirectional pin
T1IC/CR T1PWM T1EVT	T1IO1 T1IO2 T1IO3		44 43 41	46 45 44	I/O	Timer1 input capture/counter reset input pin/general-purpose bidirectional pin Timer1 pulse-width-modulation (PWM) output pin/general-purpose bidirectional pin Timer1 external event input pin/general-purpose bidirectional pin
T2AIC1/CR T2AIC2/PWM T2AEVT	T2AIO1 T2AIO2 T2AIO3		25 24 23	27 26 25	I/O	Timer2A input capture 1/counter reset input pin/general-purpose bidirectional pin Timer2A input capture 2/PWM output pin/general-purpose bidirectional pin Timer2A external event input pin/general-purpose bidirectional pin
SPISOMI SPISIMO SPICLK	SPIIO1 SPIIO2 SPIIO3		47 46 45	49 48 47	I/O	SPI slave output pin, master input pin/general-purpose bidirectional pin SPI slave input pin, master output pin/general-purpose bidirectional pin SPI bidirectional serial clock pin/general-purpose bidirectional pin

† I = input, O = output
‡ Ports A, B, C, and D can be configured only as general-purpose I/O pins. Port D3 also can be configured as SYSCLK.
NOTE 1: The three-pin configuration SCI is referred to as SCI1.

Table 1. Function A: Memory Accesses Locations for ‘x5x Devices

FUNCTION A	‘X50, ‘X52, ‘X53, AND ‘X56	‘X58	‘X59
$\overline{CSEx}$	2000h – 3FFFh (8K bytes)	A000h – BFFFh (8K bytes)	E000h – EFFFh (4K bytes)
$\overline{CSHx}$	8000h – FFFFh (32K bytes)	C000h – FFFFh (16K bytes)	F000h – FFFFh (4K bytes)
$\overline{CSPF}$	10C0h – 10FFh (64 bytes)	10C0h – 10FFh (64 bytes)	10C0h – 10FFh (64 bytes)

functional block diagram



† For the 64-pin devices, there are only six pins for port D.

description

The TMS370Cx5x family of single-chip 8-bit microcontrollers provides cost-effective real-time system control through integration of advanced peripheral function modules and various on-chip memory configurations. The TMS370Cx5x family presently consists of twenty-one devices which are grouped into seven main sub-families: the TMS370Cx50, TMS370Cx52, TMS370Cx53, TMS370Cx56, TMS370Cx58, TMS370Cx59, and SE370C75x.

The TMS370Cx5x family of devices is implemented using high-performance silicon-gate CMOS EPROM and EEPROM technologies. The low-operating power, wide-operating temperature range, and noise immunity of CMOS technology, coupled with the high performance and extensive on-chip peripheral functions, make the TMS370Cx5x devices attractive in system designs for automotive electronics, industrial motor control, computer peripheral control, telecommunications, and consumer application. Table 2 provides a memory configuration overview of the TMS370Cx5x devices.

description (continued)

Table 2. Memory Configurations

DEVICE	PROGRAM MEMORY (BYTES)		OFF-CHIP MEMORY EXP. (BYTES)	DATA MEMORY (BYTES)		OPERATING MODES		PACKAGES 68 PIN PLCC/CLCC, OR 64 PIN PSDIP/CSDIP
	ROM	EPROM		RAM	EEPROM	μC†	μP†	
TMS370Cx50: TMS370C050, TMS370C150, TMS370C250, AND TMS370C350								
TMS370C050A	4K	—	112K	256	256	√	√	FN – PLCC / NM –PSDIP
TMS370C150A	—	—	56K	256	—	—	√	FN – PLCC
TMS370C250A	—	—	56K	256	256	—	√	FN – PLCC
TMS370C350A	4K	—	112K	256	—	√	√	FN – PLCC / NM –PSDIP
TMS370Cx52: TMS370C052, TMS370C352, AND TMS370C452								
TMS370C052A	8K	—	112K	256	256	√	√	FN – PLCC / NM –PSDIP
TMS370C352A	8K	—	112K	256	—	√	√	FN – PLCC / NM –PSDIP
TMS370C452A‡	8K	—	112K	256	256	√	√	FN – PLCC
TMS370Cx53: TMS370C353								
TMS370C353A	12K	—	112K	1.5K	—	√	√	FN – PLCC
TMS370Cx56: TMS370C056, TMS370C156, TMS370C256, TMS370C356, TMS370C456, AND TMS370C756								
TMS370C056A	16K	—	112K	512	512	√	√	FN – PLCC / NM –PSDIP
TMS370C156A	—	—	56K	512	—	—	√	FN – PLCC
TMS370C256A	—	—	56K	512	512	—	√	FN – PLCC
TMS370C356A	16K	—	112K	512	—	√	√	FN – PLCC / NM –PSDIP
TMS370C456A‡	16K	—	112K	512	512	√	√	FN – PLCC
TMS370C756A	—	16K	112K	512	512	√	√	FN – PLCC / NM –PSDIP
TMS370Cx58: TMS370C058, TMS370C358, AND TMS370C758								
TMS370C058A	32K	—	64K	1K	256	√	√	FN – PLCC / NM –PSDIP
TMS370C358A	32K	—	64K	1K	—	√	√	FN – PLCC / NM –PSDIP
TMS370C758A, TMS370C758B	—	32K	64K	1K	256	√	√	FN – PLCC / NM –PSDIP
TMS370Cx59: TMS370C059 AND TMS370C759								
TMS370C059A§	48K	—	20K	3.5K	256	√	√	FN – PLCC
TMS370C759A§	—	48K	20K	3.5K	256	√	√	FN – PLCC
EPROM DEVICE: SE370C756, SE370C758, and SE370C759								
SE370C756A¶	—	16K	112K	512	512	√	√	FZ – CLCC / JN –CSDIP
SE370C758A¶, SE370C758B¶	—	32K	64K	1K	256	√	√	FZ – CLCC / JN –CSDIP
SE370C759A§¶	—	48K	20K	3.5K	256	√	√	FZ – CLCC

† μC – Microcomputer mode
μP – Microprocessor mode
‡ TMS370C45x support ROM memory security. Refer to the program ROM section.
§ Only operate up to 3 MHz SYSCLK
¶ System evaluators and development tools are for use only in a prototype environment, and their reliability has not been characterized.

description (continued)

The suffix letter (A or B) appended to the device names shown in the device column of Table 2 indicates the configuration of the device. ROM or an EPROM devices have different configurations as indicated in Table 3. ROM devices with the suffix letter A are configured through a programmable contact during manufacture.

Table 3. Suffix Letter Configuration

DEVICE†	WATCHDOG TIMER	CLOCK	LOW-POWER MODE
EPROM A	Standard	Divide-by-4 (Standard oscillator)	Enabled
EPROM B	Hard	Divide-by-1 (PLL)	Enabled
ROM A	Standard	Divide-by-4 or Divide-by-1 (PLL)	Enabled or disabled
	Hard		
	Simple		
ROM-less A	Standard	Divide-by-4	Enabled

† Refer to the “device numbering conventions” section for device nomenclature and the “device part numbers” section for ordering.

Unless otherwise noted, the terms TMS370Cx50, TMS370Cx52, TMS370Cx53, TMS370Cx56, TMS370Cx58, TMS370Cx59, and SE370C75x refer to the individual devices listed in Table 2 and described in this data sheet. All TMS370Cx5x devices contain the following on-chip peripheral modules:

- Eight-channel, 8-bit analog-to-digital converter 1 (ADC1)
- Serial communications interface 1 (SCI1)
- Serial peripheral interface (SPI)
- One 24-bit general-purpose watchdog timer
- Two 16-bit general-purpose timers (one with an 8-bit prescaler)

TMS370C756, TMS370C758, and TMS370C759 are one-time programmable (OTP) devices that are available in plastic packages. This microcomputer is effective to use for immediate production updates for other members of the TMS370Cx5x family or for low-volume production runs when the mask charge or cycle time for low-cost mask ROM devices is not practical.

The SE370C756, SE370C758, and SE370C759 have windowed ceramic packages to allow reprogramming of the program EPROM memory during the development/prototyping phase of design. The SE370C75x devices allow quick updates to breadboards and prototype systems while iterating initial designs.

The TMS370Cx5x family provides two low-power modes (STANDBY and HALT) for applications where low-power consumption is critical. Both modes stop all central processing unit (CPU) activity (that is, no instructions are executed). In the STANDBY mode, the internal oscillator and the general-purpose timer remain active. In the HALT mode, all device activity is stopped. The device retains all RAM data and peripheral configuration bits throughout both low-power modes.

The TMS370Cx5x features advanced register-to-register architecture that allows direct arithmetic and logical operations without requiring an accumulator (for example, ADD R24, R47; add the contents of register 24 to the contents of register 47 and store the result in register 47). The TMS370Cx5x family is fully instruction-set-compatible, allowing easy transition between members of the TMS370 8-bit microcontroller family.

The SPI and the two operational modes of the SCI1 give three methods of serial communications. The SCI1 allows standard RS-232-C communications interface between other common data transmission equipment, while the SPI gives high-speed communications between simpler shift-register type devices, such as display drivers, ADC1 converter, phase-locked loop (PLL), I/O expansion, or other microcontrollers in the system.

description (continued)

For large memory applications, the TMS370Cx5x family provides an external bus with non-multiplexed address and data. Precoded memory chip-select outputs can be enabled, which allows minimum-chip-count system implementations. Wait-state support facilitates performance matching among the CPU, external memory, and the peripherals. All pins associated with memory expansion interface are individually software configurable for general purpose digital input/output (I/O) pins when operating in the microcomputer mode.

The TMS370Cx5x family provides the system designer with very economical, efficient solution to real-time control applications. The TMS370 family extended development system (XDS™) and compact development tool (CDT™) solve the challenge of efficiently developing the software and hardware required to design the TMS370Cx5x into an ever-increasing number of complex applications. The application source code can be written in assembly and C-language, and the output code can be generated by the linker. The TMS370 family XDS development tools communicate through a standard RS-232-C interface with an existing personal computer. This allows the use of the personal computer editors and software utilities already familiar to the designer. The TMS370 family XDS emphasizes ease-of-use through extensive use of menus and screen windowing so that a system designer with minimal training can begin developing software. Precise real-time in-circuit emulation and extensive symbolic debug and analysis tools ensure efficient software and hardware implementation as well as reduced time-to-market cycle.

The TMS370Cx5x family together with the TMS370 family XDS/22, CDT370, design kit, starter kit, software tools, the SE370C75x reprogrammable devices, comprehensive product documentation, and customer support provide a complete solution to the needs of the system designer.

modes

The TMS370Cx5x has four operating modes, two basic modes with each mode having two memory configurations. The basic operating modes are the microcomputer and microprocessor modes, which are selected by the voltage level applied to the dedicated MC pin two cycles before $\overline{\text{RESET}}$ goes inactive. The two memory configurations then are selected through software programming of the internal system configuration registers. The four operating modes are the microcomputer single chip, microcomputer with external expansion, microprocessor without internal program memory, and microprocessor with internal program memory. These modes are described in the following list.

- Microcomputer single chip mode:
  - Operates as a self-contained microcomputer with all memory and peripherals on-chip.
  - Maximizes the general-purpose I/O capability for real-time control applications.
- Microcomputer with external expansion mode:
  - Supports bus expansion to external memory or peripherals, while all on-chip memory (RAM, ROM, EPROM, and data EEPROM) remains active.
  - Configures digital I/O ports (ports A, B, C, and D) through software, under control of the associated port control, to become external memory as follows:
    - Port A: 8-bit data memory
    - Port B and C: 16-bit address memory
    - Port D: 8-bit control memory (pin not used as function A or B can be configured as I/O)
  - Utilizes the pins available (not used for address, data, or control memory) as general-purpose input/output by programming them individually.
  - Lowers the system cost by not requiring an external address/data latch (address memory and data memory are nonmultiplexed).

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modes (continued)

- – Reduces external interface decode logic by using the precoded chip select outputs that provide direct memory/peripheral chip select or chip enable functions.
- – Function A maps up to 112K bytes of external memory into the address space by using $\overline{\text{CSE1}}$, $\overline{\text{CSE2}}$, $\overline{\text{CSH1}}$, $\overline{\text{CSH2}}$, and $\overline{\text{CSH3}}$ as memory-bank selects under software control.
- – Function B maps up to 40K bytes of external memory into the address space by using $\overline{\text{EDS}}$ under software control.

- Microprocessor without internal program memory mode:
  - – Ports A, B, C, and D (these ports are not programmable) become the address, data, and control buses for interface to external memory and peripherals.
  - – On-chip RAM and data EEPROM remain active, while the on-chip ROM or EPROM is disabled.
  - – Program area and the reset, interrupt, and trap vectors are located in off-chip memory locations.
- Microprocessor with internal program memory mode:
  - – Configured as the microprocessor without internal program memory mode with respect to the external bus interface.
  - – Application program in external memory enables the internal program ROM or EPROM to be active in the system. (Writing a zero to the MEMORY DISABLED control bit (SCCR1.2) of the SCCR1 control register accomplishes this.)

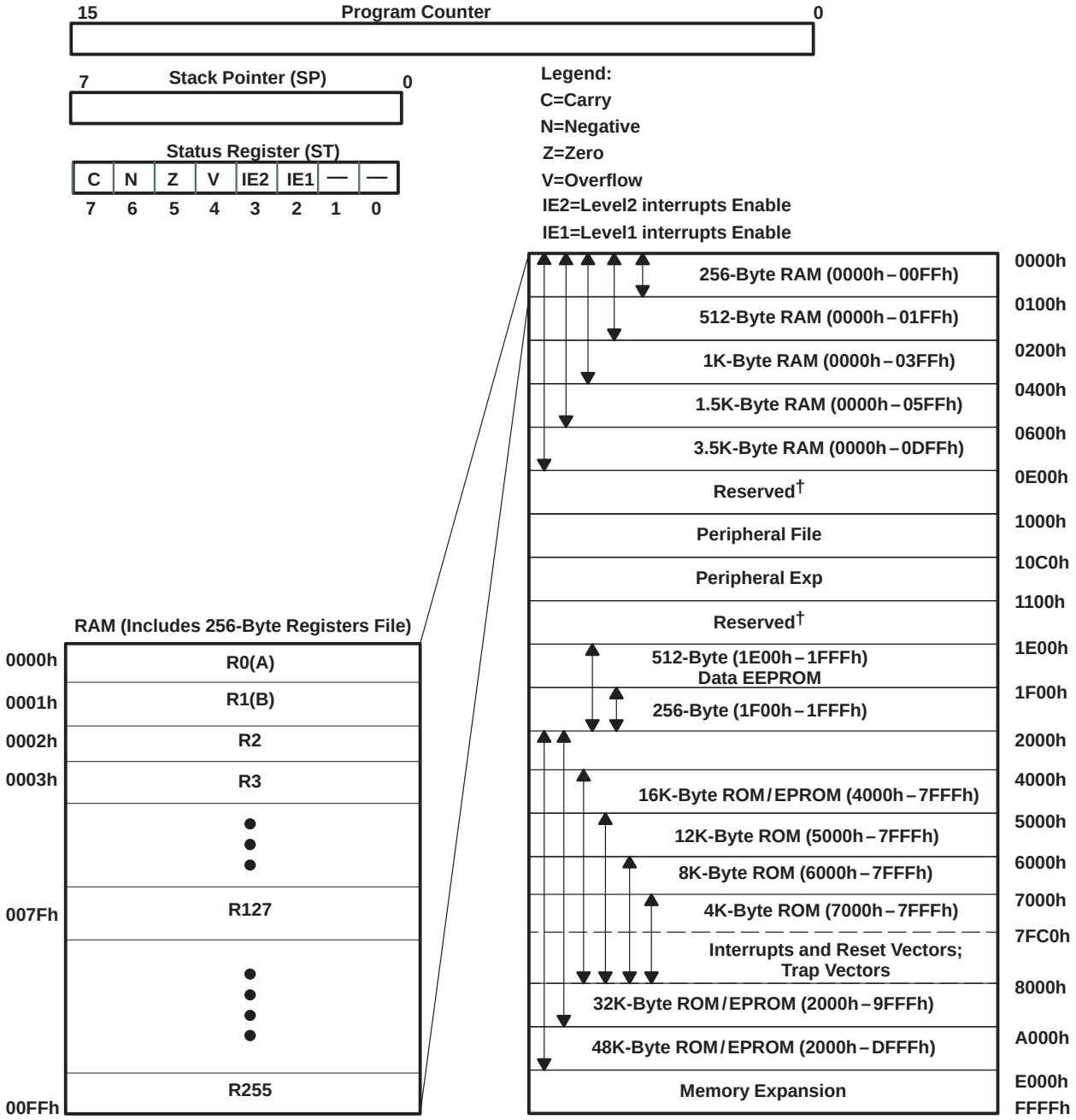
memory/peripheral wait operation

The TMS370Cx5x enhances interface flexibility by providing $\overline{\text{WAIT}}$-state support, decoupling the cycle time of the CPU from the read/write access of the external memory or peripherals. External devices can extend the read/write accesses indefinitely by placing an active low on the $\overline{\text{WAIT}}$-input pin. The CPU continues to wait as long as $\overline{\text{WAIT}}$ remains active.

Programmable automatic wait-state generation also is provided by the TMS370Cx5x on-chip bus controller. Following a hardware reset, the TMS370Cx5x is configured to add one wait state to all external bus transactions and memory and peripheral accesses automatically, thus making every external access a minimum of three system-clock cycles. The designer can disable the automatic wait-state generation if the AUTOWAIT DISABLE bit in SCCR1 is set to 1. Also, all accesses to the upper four frames of the peripheral file can be extended independently to four system clock cycles if the PF AUTO WAIT bit in SCCR0 is set to one. Programmable wait states can be used in conjunction with the external $\overline{\text{WAIT}}$ pin. In applications where the external device read/write access can interface with the TMS370Cx5x CPU using one wait state, the automatic wait-state generation can eliminate external $\overline{\text{WAIT}}$ interface logic, lowering system cost.

CPU

The CPU used on TMS370Cx5x devices is the high-performance 8-bit TMS370 CPU module. The ’x5x implements an efficient register-to-register architecture that eliminates the conventional accumulator bottleneck. The complete ’x5x instruction set is summarized in Table 23. Figure 1 illustrates the CPU registers and memory blocks.



† Reserved means the address space is reserved for future expansion.

Figure 1. Programmer’s Model

CPU (continued)

The ’x5x CPU architecture provides the following components:

- CPU registers:
  - A stack pointer that points to the last entry in the memory stack
  - A status register that monitors the operation of the instructions and contains the global-interrupt-enable bits
  - A program counter (PC) that points to the memory location of the next instruction to be executed
- A memory map that includes :
  - 256-, 512-, 1K-, 1.5K-, or 3.5K-byte general-purpose RAM that can be used for data-memory storage, program instructions, general-purpose register, or the stack (can be located only in the first 256 bytes)
  - A peripheral file that provides access to all internal peripheral modules, system-wide control functions, and EEPROM/EPROM programming control
  - 256- or 512-byte EEPROM module that provides in-circuit programmability and data retention in power-off conditions
  - 4K-, 8K-, 12K-, 16K-, 32K-, or 48K-byte ROM or 16K-, 32K-, or 48K-byte EPROM program memory

stack pointer (SP)

The SP is an 8-bit CPU register. The stack operates as a last-in, first-out, read/write memory. Typically the stack is used to store the return address on subroutine calls as well as the status-register contents during interrupt sequences.

The SP points to the last entry or to the top of the stack. The SP increments automatically before data is pushed onto the stack and decrements after data is popped from the stack. The stack can be located only in the first 256 bytes of the on-chip RAM memory.

status register (ST)

The ST monitors the operation of the instructions and contains the global-interrupt-enable bits. The ST includes four status bits (condition flags) and two interrupt-enable bits:

- The four status bits indicate the outcome of the previous instruction; conditional instructions (for example, the conditional-jump instructions) use these status bits to determine program flow.
- The two interrupt-enable bits control the two interrupt levels.

The ST register, status bit notation, and status bit definitions are shown in Table 4.

Table 4. Status Registers

7	6	5	4	3	2	1	0
C	N	Z	V	IE2	IE1	Reserved	Reserved
RW-0	RW-0	RW-0	RW-0	RW-0	RW-0		

R = read, W = write, 0 = value after reset

CPU (continued)

program counter (PC)

The contents of the PC point to the memory location of the next instruction to be executed. The PC consists of two 8-bit registers in the CPU: the program counter high (PCH) and program counter low (PCL). These registers contain the most-significant byte (MSbyte) and least-significant byte (LSbyte) of a 16-bit address.

The contents of the reset vector (7FFEh, 7FFFh) are loaded into the program counter during reset. The PCH (MSbyte of the PC) is loaded with the contents of memory location 7FFEh, and the PCL (LSbyte of the PC) is loaded with the contents of memory location 7FFFh. Figure 2 shows this operation using an example value of 6000h as the contents of memory locations 7FFEh and 7FFFh (reset vector).

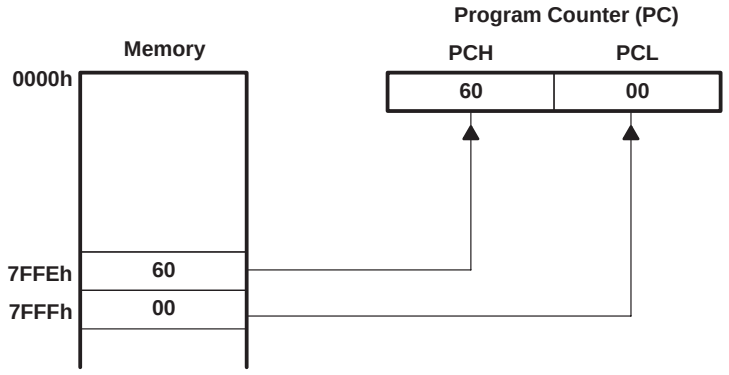


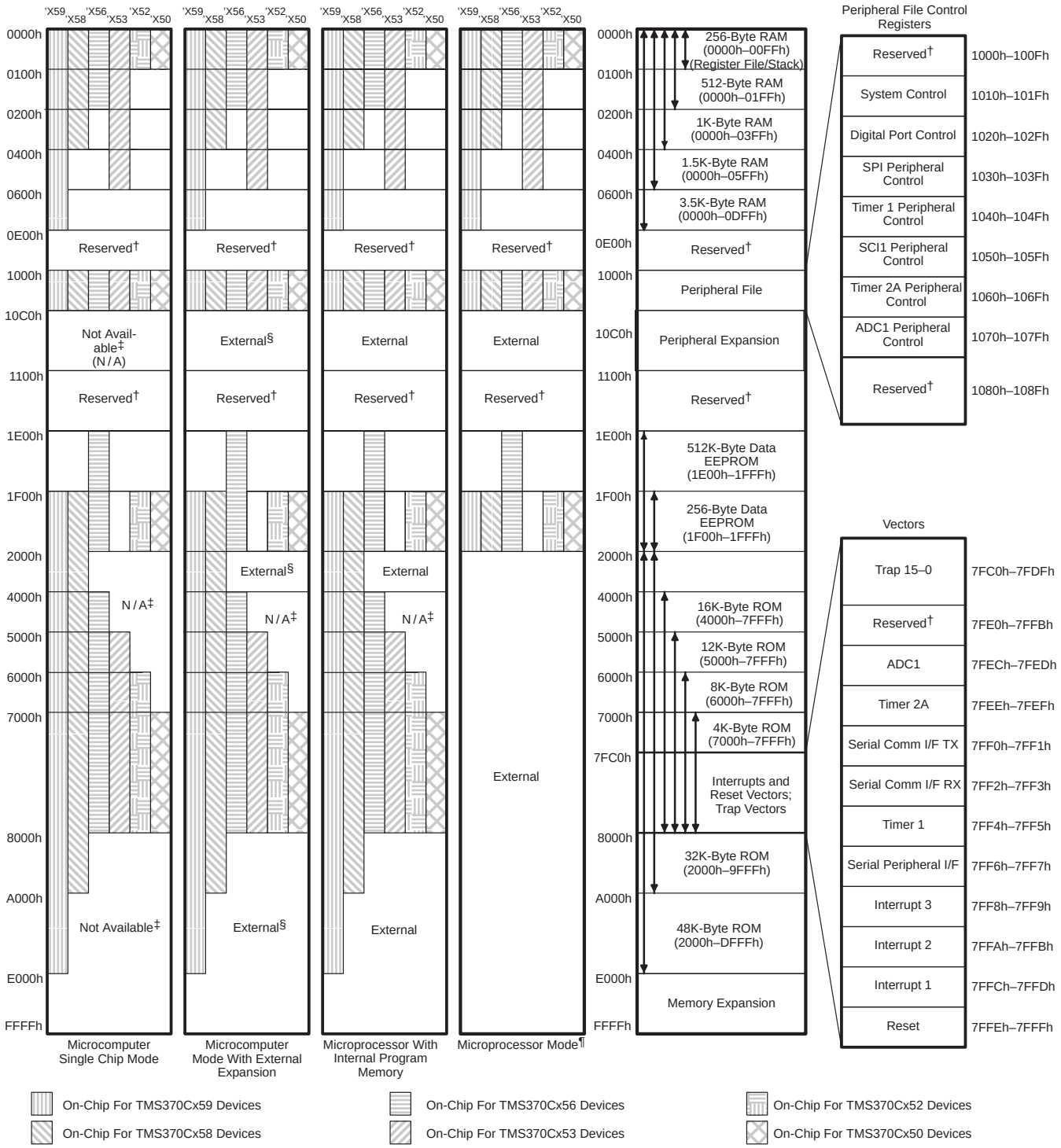
Figure 2. Program Counter After Reset

memory map

The TMS370Cx5x architecture is based on the Von Neuman architecture, where the program memory and data memory share a common address space. All peripheral input/output is memory mapped in this same common address space. In the expansion mode, external memory peripherals are also memory-mapped into this common address. As shown in Figure 3, the TMS370Cx5x provides a 16 bit-address range to access internal or external RAM, ROM, data EEPROM, EPROM input/output pins, peripheral functions, and system-interrupt vectors.

The peripheral file contains all input/output port control, on- and off-chip peripheral status and control, EPROM, EEPROM programming, and system-wide control functions. The peripheral file consists of 256 contiguous addresses located from 1000h to 10FFh. The 256 contiguous addresses are divided logically into 16 peripheral file frames of 16 bytes each. Each on-chip peripheral is assigned to a separate frame through which peripheral control and data information is passed. The TMS370Cx5x has its on-chip peripherals and system control assigned to peripheral file frames 1 through 7, addresses 1010h through 107Fh.

memory map (continued)



† Reserved = the address space is reserved for future expansion.
‡ Not available (N/A) = address space unavailable in the mode illustrated.
§ Precoded chip select outputs available on external expansion bus.
¶ Microprocessor mode is designed for ROM-less devices ('x50 and 'x56). ROM and EPROM devices can also be used in this mode but all on-chip memory is ignored.

Figure 3. TMS370Cx5x Memory Map

RAM/register file (RF)

Locations within RAM address space can serve as either register file or general-purpose read/write memory, program memory, or stack instructions. The TMS370Cx50 and TMS370Cx52 devices contain 256 bytes of internal RAM, mapped beginning at location 0000h and continuing through location 00FFh which is shown in Table 5 along with other ’x5x devices.

Table 5. RAM Memory Map

	‘x50 and ‘x52	‘x56	‘x58	‘x53	‘x59
RAM Size	256 Bytes	512 Bytes	1K Bytes	1.5K Bytes	3.5K Bytes
Memory Mapped	0000h – 00FFh	0000h – 01FFh	0000h – 03FFh	0000h – 05FFh	0000h – 0DFFh

The first 256 bytes of RAM (0000h – 00FFh) are register files, R0 through R255 (see Figure 1). The first two registers, R0 and R1, are also called register A and B, respectively. Some instructions implicitly use register A or B; for example, the instruction LDSP (load SP) assumes that the value to be loaded into the stack pointer is contained in register B. Registers A and B are the only registers cleared on reset.

peripheral file (PF)

The TMS370Cx5x control registers contain all the registers necessary to operate the system and peripheral modules on the device. The instruction set includes some instructions that access the PF directly. These instructions designate the register by the number of the PF relative to 1000h, preceded by P0 for a hexadecimal designator or by P for a decimal designator. For example, the system control register 0 (SCCR0) is located at address 1010h; its peripheral file hexadecimal designator is P010, and its decimal designator is P16. Table 6 shows the TMS370Cx5x peripheral files.

Table 6. TMS370Cx5x Peripheral File Address map

ADDRESS RANGE	PERIPHERAL FILE DESIGNATOR	DESCRIPTION
1000h – 100Fh	P000 – P00F	Reserved for factory test
1010h – 101Fh	P010 – P01F	System and EEPROM/EPROM control registers
1020h – 102Fh	P020 – P02F	Digital I/O port control registers
1030h – 103Fh	P030 – P03F	Serial peripheral interface registers
1040h – 104Fh	P040 – P04F	Timer 1 registers
1050h – 105Fh	P050 – P05F	Serial communication interface 1 registers
1060h – 106Fh	P060 – P06F	Timer 2A registers
1070h – 107Fh	P070 – P07F	Analog-to-digital converter 1 registers
1080h – 10BFh	P080 – P0BF	Reserved
10C0h – 10FFh	P0C0 – P0FF	External peripheral control

data EEPROM

The TMS370Cx56 devices contain 512 bytes of data EEPROM, which are memory mapped beginning at location 1E00h and continuing through location 1FFFh as shown in Table 7 along with other ‘x5x devices.

Table 7. Data-EEPROM Memory Map

	‘x50, ‘x52, ‘x58, and ‘x59	‘x56	‘X53
Data-EEPROM Size	256 Bytes	512 Bytes	None
Memory Mapped	1F00h – 1FFFh	1E00h – 1FFFh	None

data EEPROM (continued)

Writing to the data EEPROM module is controlled by the data EEPROM control register (DEECTL) and the write-protection register (WPR). Programming algorithm examples are available in the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B). The data EEPROM features include the following:

- Programming:
  - Bit, byte, and block write/erase modes
  - Internal charge pump circuitry. No external EEPROM programming voltage supply is needed.
  - Control register: Data EEPROM programming is controlled by the data EEPROM control register (DEECTL) located in the PF frame beginning at location P01A.
  - In-circuit programming capability: There is no need to remove the device to program it.
- Write-protection: Writes to the data EEPROM are disabled during the following conditions:
  - Reset: All programming of the data EEPROM module is halted.
  - Write protection active: There is one write-protect bit per 32-byte EEPROM block.
  - Low-power mode operation
- Write protection can be overridden by applying 12 V to MC.

Table 8 shows the memory map of the control registers.

Table 8. Data EEPROM and Program EPROM Control Registers Memory Map

ADDRESS	SYMBOL	NAME
P014	EPCTLH	Program EPROM control register – high array
P015 – P016		Reserved
P017	INT1	External interrupt 1 control register
P018	INT2	External interrupt 2 control register
P019	INT3	External interrupt 3 control register
P01A	DEECTL	Data EEPROM control register
P01B		Reserved
P01C	EPCTLM	Program EPROM control register – middle array
P01D		Reserved
P01E	EPCTLL	Program EPROM control register – low array

For the 16K-byte EPROM device, program memory is controlled by P01C; for the 32K-byte EPROM device, the program memory is controlled by P01C and P01E; for the 48K-byte EPROM device, the program memory is controlled by P014, P01C, and P01E.

program EPROM

The '370C756 consists of a 16K-byte array of EPROM at address locations 4000h through 7FFFh. The '370C758 consists of 32K bytes made up of two 16K-byte arrays of EPROM; the first 16K-bytes array is located at address locations 2000h through 5FFFh, and the second 16K byte array is located at address locations 6000h through 9FFFh. The '370C759 consists of 48K bytes that is made up of three 16K byte arrays of EPROM; the first 16K bytes array is located at address locations 2000h through 5FFFh, the second 16K-byte array is located at address locations 6000h through 9FFFh, the third 16K-byte array is located at address locations A000h through DFFFh (see Figure 3).

program EPROM (continued)

The EPROM memory map in Table 9 expresses the following:

- The programming control register for program EPROM (EPCTLM) for 16K-byte EPROM is located at address 101Ch (P01C).
- For the 32K-byte EPROM, the first 16K-byte array is controlled by EPCTLL, located at 101Eh (P01E); the second 16K-byte array is controlled by EPCTLM, located at 101Ch (P01C).
- For the 48K-byte EPROM, the first 16K-byte array is controlled by EPCTLL, located at 101Eh (P01E); the second 16K-byte array is controlled by EPCTLM, located at 101Ch (P01C); the third 16K-byte array is controlled by EPCTLH, located at 1014h (P014).

Table 9. EPROM Memory Map

	’756	’758		’759		
EPROM size	16K Bytes	32K Bytes		48K Bytes		
Memory Mapped	16K 4000h – 7FFFh	First 16K 2000h – 5FFFh	Second 16K 6000h – 9FFFh	First 16K 2000h – 5FFFh	Second 16K 6000h – 9FFFh	Third 16K A000h – DFFFh
Contol Registers	EPCTLM P01C	EPCTLL P01E	EPCTLM P01C	EPCTLL P01E	EPCTLM P01C	EPCTLH P014

Reading the program-EPROM modules is identical to reading other internal memory. During programming, the EPROM is controlled by the EPCTL. The program EPROM modules’ features include:

- Programming
  - In-circuit programming capability if V_{PP} is applied to MC
  - Control register: Program EPROM programming is controlled by the program EPROM control registers (EPCTLL, EPCTLM, and EPCTLH) located in the PF frame as shown in Table 8.
  - Programming one EPROM module while executing the other
- Write protection: Writes to the program EPROM are disabled under the following conditions:
  - Reset: All programming to the EPROM module is halted.
  - Low-power modes
  - 13 V not applied to MC

program ROM

The program ROM consists of 4K to 48K bytes of mask-programmable ROM. The program ROM is used for permanent storage of data or instructions. Programming of the mask ROM is performed at the time of device fabrication. ROM security is a feature of the ‘45x devices, which inhibits reading of the data using the programmer.

Table 10. ROM Memory Map†

	‘x50	‘x52	‘x53	‘x56	‘x58	‘x59
ROM Size	4K Bytes	8K Bytes	12K Bytes	16K Bytes	32K Bytes	48K Bytes
Memory Mapped	7000h – 7FFFh	6000h – 7FFFh	5000h – 7FFFh	4000h – 7FFFh	3000h – 9FFFh	2000h – DFFFh

† Memory addresses 7FE0h through 7FEBh are reserved for Texas Instruments (TI™), and addresses 7FECh through 7FFFh are reserved for interrupt and reset vectors. Trap vectors, used with TRAP0 through TRAP15 instructions are located between addresses 7FC0h and 7FDFh.

TI is a trademark of Texas Instruments Incorporated.

system reset

The system-reset operation ensures an orderly start-up sequence for the TMS370Cx5x CPU-based device. There are up to three different actions that can cause a system reset to the device. Two of these actions are internally generated, while one ($\overline{\text{RESET}}$) is controlled externally. These actions are as follows:

- Watchdog (WD) timer. A watchdog-generated reset occurs if an improper value is written to the WD key register, or if the re-initialization does not occur before the watchdog timer timeout . See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.
- Oscillator reset. Reset occurs when the oscillator operates outside the recommended operating range. See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.
- External $\overline{\text{RESET}}$ Pin. A low-level signal can trigger an external reset. To ensure a reset, the external signal should be held low for one SYSCLK cycle. Signals of less than one SYSCLK can generate a reset. See the *TMS370 User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B) for more information.

Once a reset source is activated, the external $\overline{\text{RESET}}$ pin is driven (active) low for a minimum of eight SYSCLK cycles. This allows the 'x5x device to reset external system components. Additionally, if a cold-start condition (V_{CC} is off for several hundred milliseconds) occurs, oscillator failure occurs, or $\overline{\text{RESET}}$ pin is held low, then the reset logic holds the device in a reset state for as long as these actions are active.

After a reset, the program can check the oscillator fault flag (OSC FLT FLAG, SCCR0.4), the cold start flag (COLD START, SCCR0.7), and the watchdog reset (WD OVRFL INT FLAG, T1CTL2.5) to determine the source of the reset. A reset does not clear these flags. Table 11 lists the reset sources.

Table 11. Reset Sources

REGISTER	ADDRESS	PF	BIT NO.	CONTROL BIT	SOURCE OF RESET
SCCR0	1010h	P010	7	COLD START	Cold (power-up)
SCCR0	1010h	P010	4	OSC FLT FLAG	Oscillator out of range
T1CTL2	104Ah	P04A	5	WD OVRFL INT FLAG	Watchdog timer timeout

Once a reset is activated, the following sequence of events occurs:

1. The CPU registers initialize: ST = 00h, SP = 01h (reset state).
2. Registers A and B initialize to 00h (no other RAM is changed).
3. The contents of the LSbyte of the reset vector (07FFh) are read and stored in the PCL.
4. The contents of the MSbyte of the reset vector (07FEh) are read and stored in the PCH.
5. Program execution begins with an opcode fetch from the address pointed to by the PC.

The reset sequence takes 20 SYSCLK cycles from the time the reset pulse is released until the first opcode fetch. During a reset, RAM contents (except for registers A and B) remain unchanged, and the module control register bits are initialized to their reset state. During $\overline{\text{RESET}}$, the two basic operating modes which are the microcomputer and microprocessor modes can be selected by applying the desired voltage level to the dedicated MC pin two cycles before $\overline{\text{RESET}}$ goes inactive (refer to page 7 for operating modes description).

interrupts

The TMS370 family software-programmable interrupt structure permits flexible on-chip and external interrupt configurations to meet real-time interrupt-driven application requirements. The hardware interrupt structure incorporates two priority levels as shown in Figure 4. Interrupt level 1 has a higher priority than interrupt level 2. The two priority levels can be masked independently by the global interrupt mask bits (IE1 and IE2) of the status register.

Each system interrupt is configured independently to either the high- or low-priority chain by the application program during system initialization. Within each interrupt chain, the interrupt priority is fixed by the position of the system interrupt. However, since each system interrupt is configured selectively on either the high- or low-priority interrupt chain, the application program can elevate any system interrupt to the highest priority. Arbitration between the two priority levels is performed within the CPU. Arbitration within each of the priority chains is performed within the peripheral modules to support interrupt expansion for future modules. Pending interrupts are serviced upon completion of current instruction execution, depending on their interrupt mask and priority conditions.

The TMS370Cx5x has nine hardware system interrupts (plus $\overline{\text{RESET}}$) as shown in Table 12. Each system interrupt has a dedicated vector located in program memory through which control is passed to the interrupt service routines. A system interrupt can have multiple interrupt sources (e.g., SCI RXINT has two interrupt sources). All of the interrupt sources are individually maskable by local interrupt-enable control bits in the associated PF. Each interrupt source FLAG bit is individually readable for software polling or determining which interrupt source generated the associated system interrupt. Interrupt control block diagram is illustrated in Figure 4.

interrupts (continued)

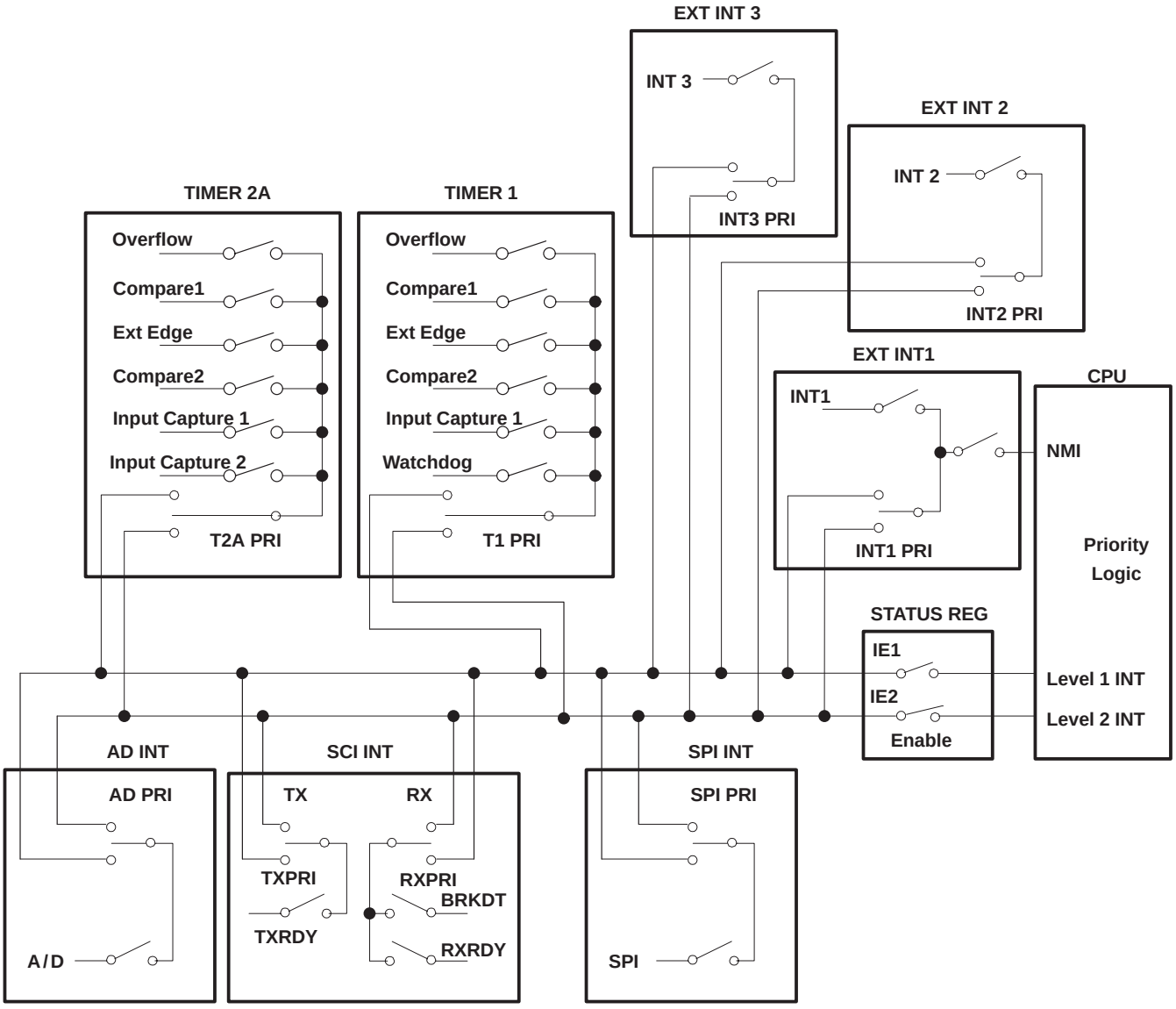


Figure 4. Interrupt Control

On-chip peripheral functions generate six of the system interrupts. Three external interrupts also are supported. Software configuration of the external interrupts is performed through the INT1, INT2, and INT3 control registers in PF frame 1. Each external interrupt is individually software configurable for input polarity (rising or falling edge) for ease of system interface. External interrupt INT1 is software configurable as either a maskable or non-maskable interrupt. When INT1 is configured as nonmaskable, it cannot be masked by the individual- or global-enable mask bits. The INT1 NMI bit is protected during non-privileged operation and, therefore, should be configured during the initialization sequence following reset. To maximize pin flexibility, external interrupts INT2 and INT3 can be software configured as general purpose input/output pins if the interrupt function is not required (INT1 can be similarly configured as an input pin). Table 12 shows the interrupt vector sources, corresponding addresses, and hardware priorities.

interrupts (continued)

Table 12. Hardware System Interrupts

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	VECTOR ADDRESS	PRIORITY†
External $\overline{\text{RESET}}$ Watchdog overflow Oscillator fault detect	COLD START WD OVRFL INT FLAG OSC FLT FLAG	$\overline{\text{RESET}}$‡	7FFEh, 7FFFh	1
External INT1	INT1 FLAG	INT1‡	7FFCh, 7FFDh	2
External INT2	INT2 FLAG	INT2‡	7FFAh, 7FFBh	3
External INT3	INT3 FLAG	INT3‡	7FF8h, 7FF9h	4
SPI RX/TX complete	SPI INT FLAG	SPIINT	7FF6h, 7FF7h	5
Timer 1 overflow Timer 1 compare 1 Timer 1 compare 2 Timer 1 external edge Timer 1 input capture 1 Watchdog overflow	T1 OVRFL INT FLAG T1C1 INT FLAG T1C2 INT FLAG T1EDGE INT FLAG T1IC1 INT FLAG WD OVRFL INT FLAG	T1INT§	7FF4h, 7FF5h	6
SCI RX data register full SCI RX break detect	RXRDY FLAG BRKDT FLAG	RXINT‡	7FF2h,7FF3h	7
SCI TX data register empty	TXRDY FLAG	TXINT	7FF0h, 7FF1h	8
Timer 2A overflow Timer 2A compare 1 Timer 2A compare 2 Timer 2A external edge Timer 2A input capture 1 Timer 2A input capture 2	T2A OVRFL INT FLAG T2AC1 INT FLAG T2AC2 INT FLAG T2AEDGE INT FLAG T2AIC1 INT FLAG T2AIC2 INT FLAG	T2AINT	7FEEh, 7FEFh	9
A/D conversion complete	AD INT FLAG	ADINT	7FECh, 7FEDh	10

† Relative priority within an interrupt level
‡ Releases microcontroller from STANDBY and HALT low-power modes.
§ Releases microcontroller from STANDBY low-power mode.

privileged operation and EEPROM write-protection override

The TMS370Cx5x family has significant flexibility to enable the designer to software-configure the system and peripherals to meet the requirements of a broad variety of applications. The nonprivileged mode of operation ensures the integrity of the system configuration, once it is defined for an application. Following a hardware reset, the TMS370Cx5x operates in the privileged mode, where all peripheral file registers have unrestricted read/write access, and the application program configures the system during the initialization sequence following reset. As the last step of system initialization, the PRIVILEGE DISABLE bit (SCCR2.0) should be set to 1 to enter the nonprivileged mode; disabling write operations to specific configuration control bits within the peripheral file. Table 13 displays the system configuration bits that are write-protected during the nonprivileged mode and must be configured by software prior to exiting the privileged mode.

privileged operation and EEPROM write-protection override (continued)

Table 13. Privileged Bits

REGISTER†		CONTROL BIT
NAME	LOCATION	
SCCRO	P010.5 P010.6	PF AUTOWAIT OSC POWER
SCCR1	P011.2 P011.4	MEMORY DISABLE AUTOWAIT DISABLE
SCCR2	P012.0 P012.1 P012.3 P012.4 P012.6 P012.7	PRIVILEGE DISABLE INT1 NMI CPU STEST BUS STEST PWRDWN/IDLE HALT/STANDBY
SPIPRI	P03F.5 P03F.6 P03F.7	SPI ESPEN SPI PRIORITY SPI STEST
SCIPRI	P05F.4 P05F.5 P05F.6 P05F.7	SCI ESPEN SCIRX PRIORITY SCITX PRIORITY SCI STEST
T1PRI	P04F.6 P04F.7	T1 PRIORITY T1 STEST
T2APRI	P06F.6 P06F.7	T2A PRIORITY T2A STEST
ADPRI	P07F.5 P07F.6 P07F.7	AD ESPEN AD PRIORITY AD STEST

† The privileged bits are shown in a bold typeface in Table 15.

The write-protect override (WPO) mode provides an external hardware method for overriding the write-protection registers of data EEPROM on the TMS370Cx5x. The WPO mode is entered by applying a 12-V input to MC after $\overline{\text{RESET}}$ input goes high (logic 1). The high voltage on MC during the WPO mode is not the programming voltage for the data EEPROM or Program EPROM. All EEPROM programming voltages are generated on-chip. The WPO mode provides hardware system-level capability to modify the content of the data EEPROM while the device remains in the application, but only while requiring a 12-V external input on the MC pin (normally not available in the end application except in a service or diagnostic environment).

low-power and IDLE modes

The TMS370Cx5x devices have two low-power modes (STANDBY and HALT) and an IDLE mode. For mask-ROM devices, low-power modes can be disabled permanently through a programmable contact at the time when the mask is manufactured.

The STANDBY and HALT low power modes significantly reduce power consumption by reducing or stopping the activity of the various on-chip peripherals when processing is not required. Each of the low-power modes is entered by executing the IDLE instruction when the PWRDWN/IDLE bit in SCCR2 has been set to 1. The HALT/STANDBY bit in SCCR2 controls which low-power mode is entered.

In the STANDBY mode (HALT/STANDBY = 0), all CPU activity and most peripheral module activity is stopped; however, the oscillator, internal clocks, timer 1, and the receive start-bit detection circuit of the serial communications interface remain active. System processing is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$, external interrupt on INT1, INT2, INT3, timer 1 interrupt, or low level on the receive pin of the serial communications interface 1) is detected.

low-power and IDLE modes (continued)

In the HALT mode (HALT/STANDBY = 1), the TMS370Cx5x is placed in its lowest power consumption mode. The oscillator and internal clocks are stopped, causing all internal activity to be halted. System activity is suspended until a qualified interrupt (hardware $\overline{\text{RESET}}$, external interrupt on the INT1, INT2, INT3, or low level on the receive pin of the serial communications interface 1) is detected. The low-power mode selection bits are summarized in Table 14.

Table 14. Low-Power/Idle Control Bits

POWER-DOWN CONTROL BITS		MODE SELECTED
PWRDWN/IDLE (SCCR2.6)	HALT/STANDBY (SCCR2.7)	
1	0	STANDBY
1	1	HALT
0	X	IDLE

X = don't care

When low-power modes are disabled through a programmable contact in the mask-ROM devices, writing to the SCCR2.6–7 bits is ignored. In addition, if an idle instruction is executed when low-power modes are disabled through a programmable contact, the device always enters the IDLE mode.

To provide a method of always exiting low-power modes for mask-ROM devices, INT1 is enabled automatically as a nonmaskable interrupt (NMI) during low-power modes when the hard watchdog mode is selected. This means that the NMI is generated always, regardless of the interrupt enable flags.

The following information is preserved throughout both the STANDBY and HALT modes: RAM (register file), CPU registers (stack pointer, program counter, and status register), I/O pin direction and output data, and status registers of all on-chip peripheral functions. Since all CPU instruction processing is stopped during the STANDBY and HALT modes, the clocking of the watchdog timer is inhibited.

clock modules

The 'x5x family provides two clock options which are referred to as divide-by-1 (PLL) and divide-by-4 (standard oscillator). Both the divide-by-1 and divide-by-4 options are configurable during the manufacturing process of a TMS370 microcontroller. The 'x5x ROM-masked devices offer both options to meet system engineering requirements. Only one of the two clock options is allowed on each ROM device. The '75xA EPROM has only the standard divide-by-4, while the '75xB EPROM has the divide-by-1.

The divide-by-1 clock module option provides the capability for reduced electromagnetic interference (EMI) with no added cost.

The divide-by-1 provides a 1-to-1 match of the external resonator frequency to the internal system clock (SYSCLK) frequency. The divide-by-4 produces a SYSCLK which is one-fourth the frequency of the external resonator. Inside the divide-by-1 module, the frequency of the external resonator is multiplied by four. The clock module then divides the resulting signal by four to provide the four-phased internal system clock signals. The resulting SYSCLK is equal to the resonator frequency. The frequencies are formulated as follows

$$\text{Divide-by-4 option : SYSCLK} = \frac{\text{external resonator frequency}}{4} = \frac{\text{CLKIN}}{4}$$

$$\text{Divide-by-1 option : SYSCLK} = \frac{\text{external resonator frequency} \times 4}{4} = \text{CLKIN}$$

The main advantage of choosing a divide-by-1 oscillator is the improved EMI performance. The harmonics of low-speed resonators extend through less of the emissions spectrum than the harmonics of faster resonators. The divide-by-1 provides the capability of reducing the resonator speed by four times, and this results in a steeper decay of emissions produced by the oscillator.

system configuration registers

Table 15 contains system configuration and control functions and registers for controlling EEPROM programming. The privileged bits are shown in a bold typeface and shaded.

Table 15. Peripheral File Frame 1: System Configuration Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P010	COLD START	**OSC POWER**	**PF AUTO WAIT**	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	µP/µC MODE	SCCR0
P011	—	—	—	**AUTOWAIT DISABLE**	—	**MEMORY DISABLE**	—	—	SCCR1
P012	**HALT/ STANDBY**	**PWRDWN/ IDLE**	—	**BUS STEST**	**CPU STEST**	—	**INT1 NMI**	**PRIVILEGE DISABLE**	SCCR2
P013	Reserved								
P014	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLH
P015 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLM
P01D	Reserved								
P01E	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLL
P01F	Reserved								

digital port control registers

Peripheral file frame 2 contains the digital I/O pin configuration and control registers. Table 16 lists the specific addresses, registers, and control bits within this peripheral file frame.

Table 16. Peripheral File Frame 2: Digital Port Control Registers

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P020	Reserved								APORT1
P021	Port A Control Register 2								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	Port C Control Register 2								CPORT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1								DPORT1
P02D	Port D Control Register 2†								DPORT2
P02E	Port D Data								DDATA
P02F	Port D Direction								DDIR

† To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

digital port control registers (continued)

Table 17. Port Configuration Register Setup

PORT	PIN	INPUT	OUTPUT	FUNCTION A	FUNCTION B (μP MODE)
		XPORT1 = 0† XPORT2 = 0 XDATA = y XDIR = 0	XPORT1 = 0† XPORT2 = 0 XDATA = q XDIR = 1	XPORT1 = 0† XPORT2 = 1 XDATA = x XDIR = x	XPORT1 = 1† XPORT2 = 1 XDATA = x XDIR = x
A	0–7	Data In y	Data Out q	Data Bus	Reserved
B	0–7	Data In y	Data Out q	Low ADDR	Reserved
C	0–7	Data In y	Data Out q	Hi ADDR	Reserved
D	0 1 2 3 4 5 6 7	Data In y	Data Out q	$\overline{CSE2}$ $\overline{CSH3}$ CSH2 SYSCLK R/$\overline{W}$ $\overline{CSPF}$ $\overline{CSH1}$ CSE1	$\overline{OCF}$ — — SYSCLK R/$\overline{W}$ — $\overline{EDS}$ $\overline{WAIT}$
XPORT1 = 1 XPORT2 =0 XDATA = x XDIR = x				Not defined	

† DPORT only

timer 1 module

The programmable timer 1 (T1) module of the TMS370Cx5x provides the designer with the enhanced timer resources required to perform realtime system control. The T1 module contains the general-purpose timer and the watchdog (WD) timer. The two independent 16-bit timers (T1 and WD) allow program selection of input clock sources (real-time, external event, or pulse-accumulate) with multiple 16-bit registers (input capture and compare) for special timer function control. The T1 module includes three external device pins that can be used for multiple counter functions (operation mode dependent) or used as general-purpose I/O pins. T1 module is shown in Figure 5.

timer 1 module (continued)

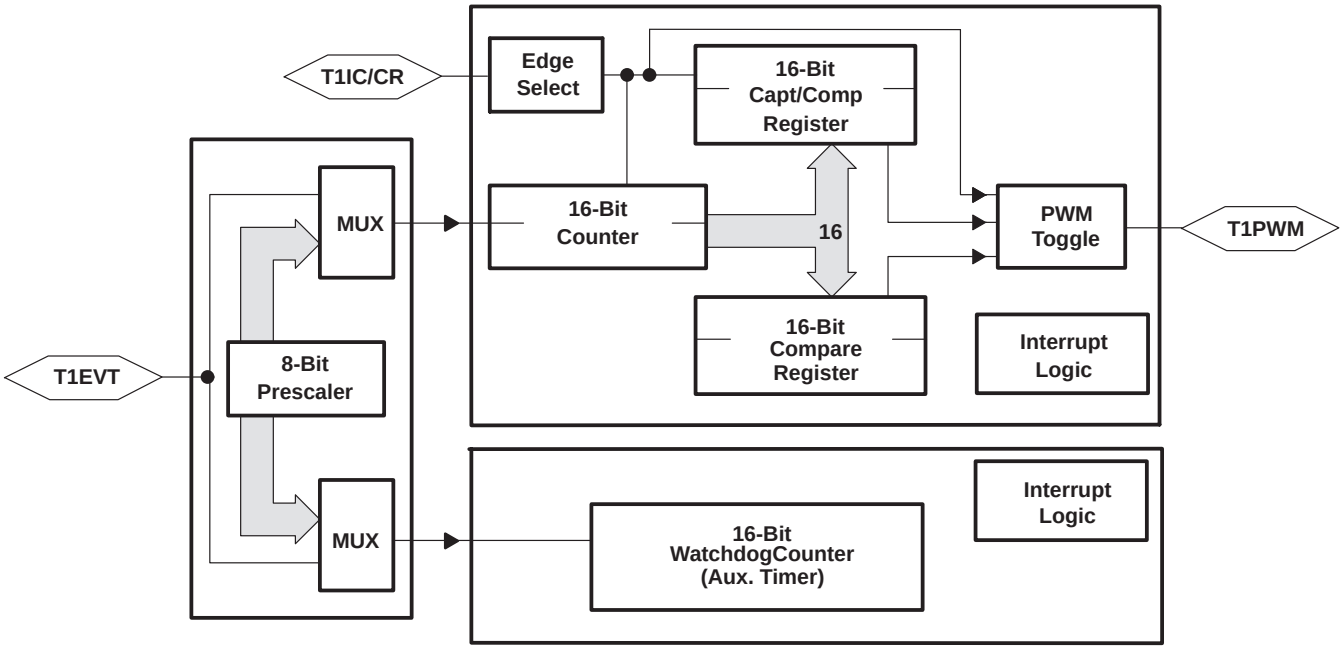


Figure 5. Timer 1 Block Diagram

- Three T1 I/O pins:
  - T1IC/CR: T1 input capture / counter reset input pin, or general-purpose bidirectional I/O pin
  - T1PWM: T1 pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
  - T1EVT: T1 event input pin, or general-purpose bidirectional I/O pin
- Two operation modes:
  - Dual-compare mode: Provides PWM signal
  - Capture/compare mode: Provides input capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register
- One 16-bit WD counter can be used as an event counter, a pulse accumulator, or an interval timer if watchdog feature is not needed.
- Prescaler/clock sources that determine one of eight clock sources for general-purpose timer
- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T1IC/CR)

timer 1 module (continued)

- Interrupts that can be generated on the occurrence of:
  - A capture
  - A compare equal
  - A counter overflow
  - An external edge detection
- Sixteen T1 module control registers located in the PF frame, beginning at address P040

Table 18 shows the T1 module control register.

Table 18. T1 Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Modes: Dual-Compare and Capture/Compare								
P040	Bit 15	T1 Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare Register LSbyte						Bit 0	
P044	Bit 15	Capture/Compare Register MSbyte						Bit 8	T1CC
P045	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P046	Bit 15	Watchdog Counter MSbyte						Bit 8	WDCNTR
P047	Bit 7	Watchdog Counter LSbyte						Bit 0	
P048	Bit 15	Watchdog Reset Key						Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
	Mode: Dual-Compare								
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
	Mode: Capture/Compare								
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
	Modes: Dual-Compare and Capture/Compare								
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	**T1 STEST**	**T1 PRIORITY**	—	—	—	—	—	—	T1PRI

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to the simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

timer 1 module (continued)

The T1 capture/compare mode block diagram is illustrated in Figure 6. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

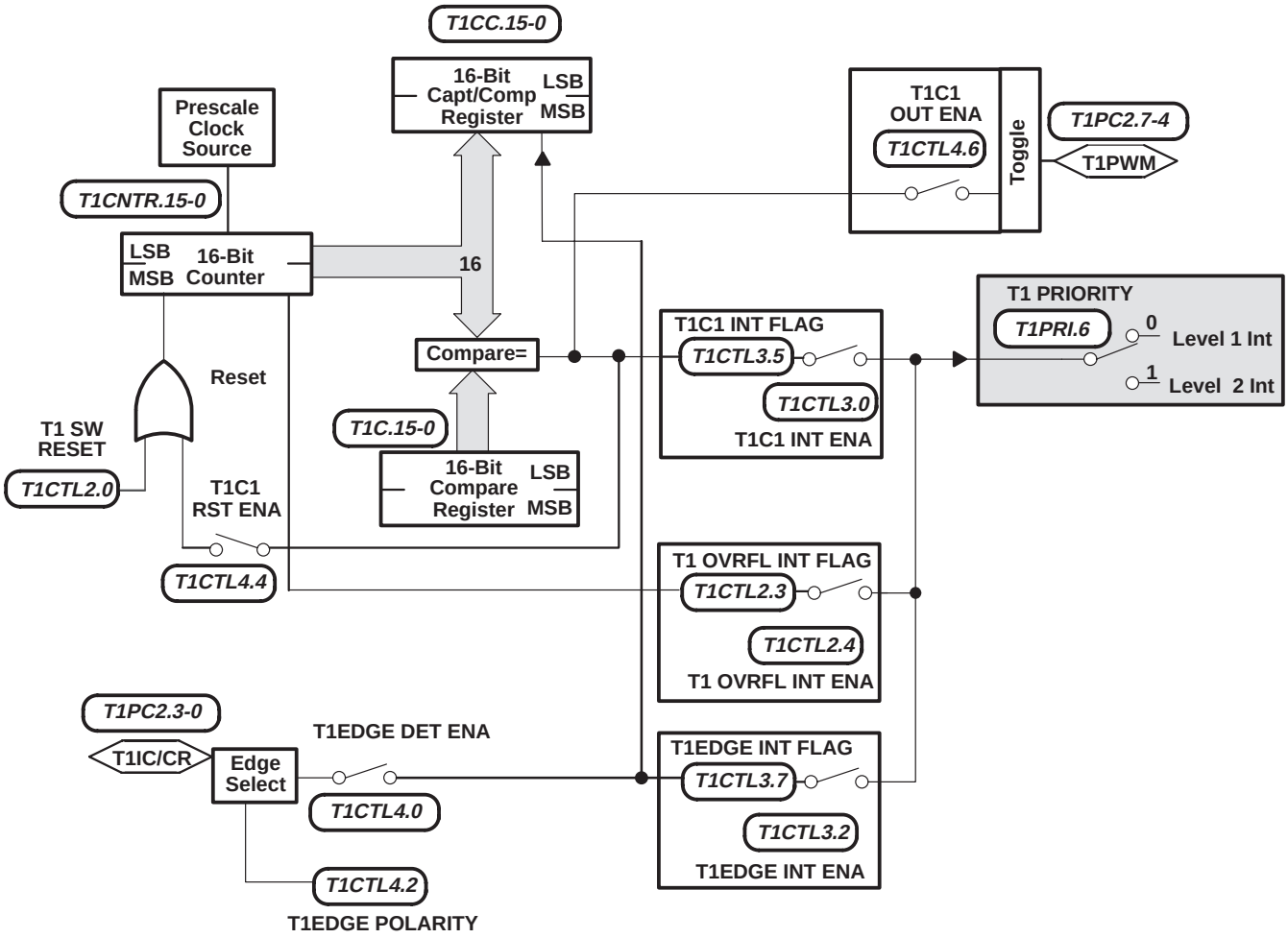


Figure 6. Capture/Compare Mode

timer 1 module (continued)

The T1 dual-compare mode block diagram is illustrated in Figure 7. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T1CTL2.0 is 104Ah, bit 0, in the T1CTL2 register.

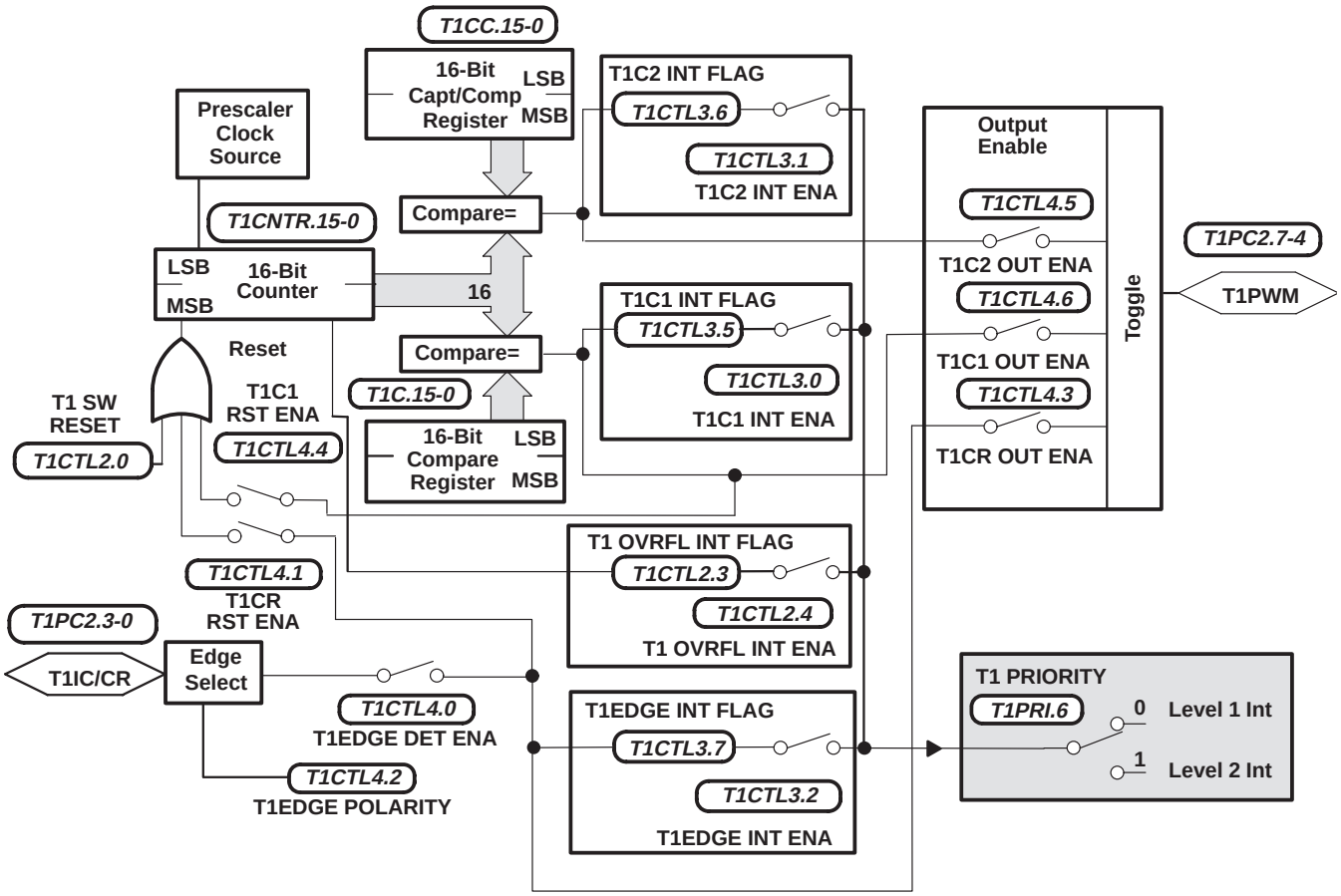


Figure 7. Dual-Compare Mode

timer 1 module (continued)

The TMS370Cx5x device includes a 24-bit watchdog (WD) timer, contained in the T1 module, which can be software-programmed as an event counter, pulse accumulator, or interval timer if the watchdog function is not desired. The WD function is to monitor software and hardware operation and to implement a system reset when the WD counter is not serviced properly (WD counter overflow or WD counter is reinitialized by an incorrect value). The WD can be configured as one of the three mask options: standard watchdog, hard watchdog, or simple counter.

- Standard watchdog configuration (see Figure 8) – for ’C75xA EPROM and mask-ROM devices
  - Watchdog mode
    - Ten different WD overflow rates ranging from 6.55 ms to 3.35 s at 5-MHz SYSCLK
    - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
    - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
    - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset
  - Non-watchdog mode
    - Watchdog timer can be configured as an event counter, pulse accumulator, or an interval timer

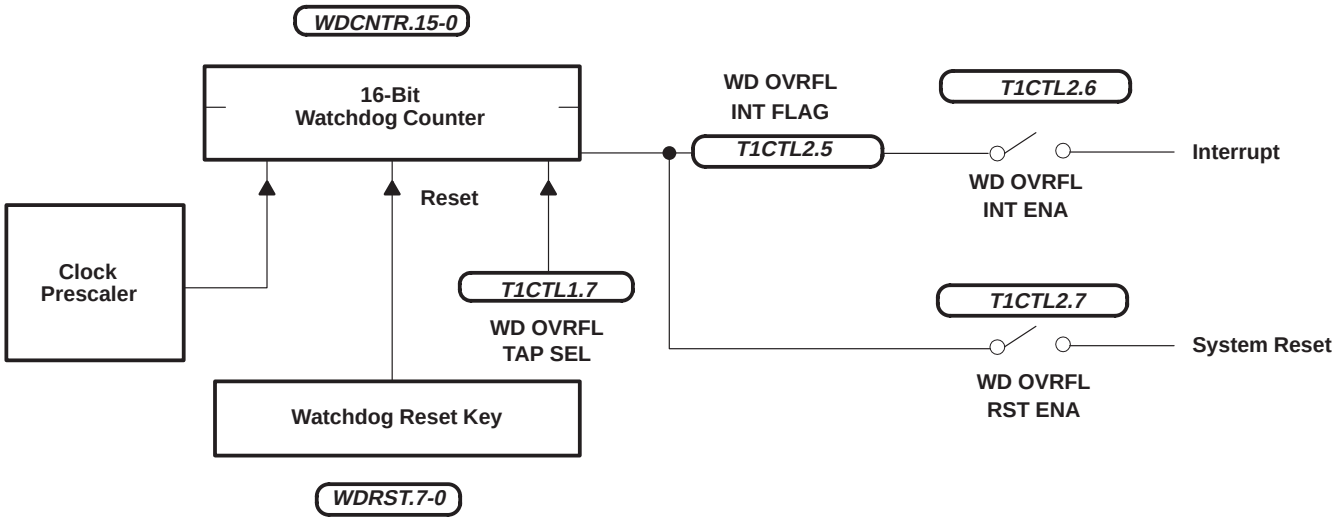


Figure 8. Standard Watchdog

timer 1 module (continued)

- Hard watchdog configuration (see Figure 9) – for ‘C75xB EPROM and mask-ROM devices
  - Eight different WD overflow rates ranging from 26.2 ms to 3.35 s at 5-MHz SYSCLK.
  - A WD reset key (WDRST) register is used to clear the watchdog counter (WDCNTR) when a correct value is written.
  - Generates a system reset if an incorrect value is written to the watchdog reset key or if the counter overflows
  - Automatic activation of the WD timer upon power-up reset
  - INT1 is enabled as nonmaskable interrupt during low-power modes
  - A watchdog overflow flag (WD OVRFL INT FLAG) bit that indicates whether the WD timer initiated a system reset

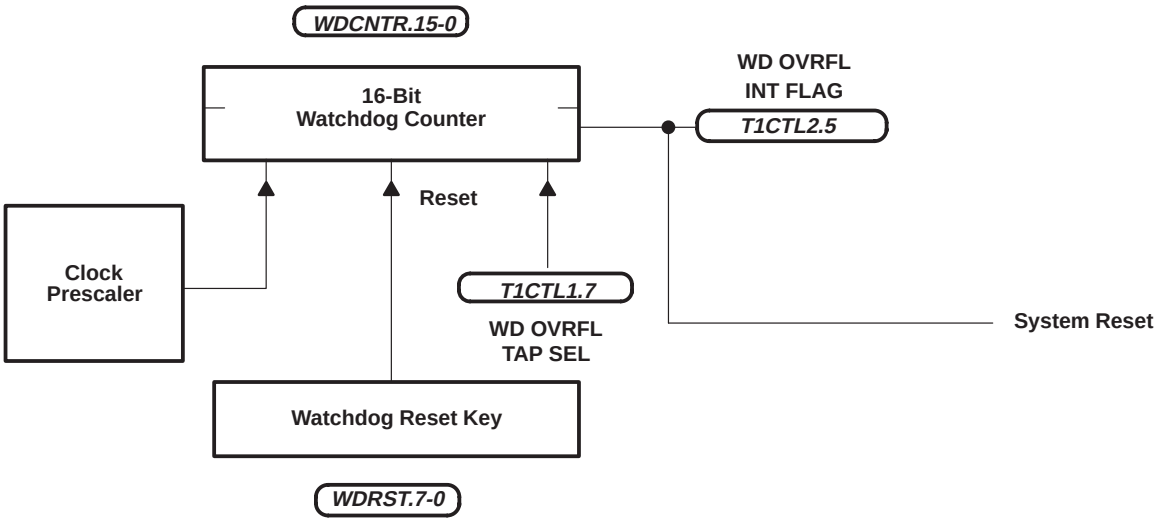


Figure 9. Hard Watchdog

timer 1 module (continued)

- Simple-counter configuration (see Figure 10) – for mask-ROM devices only
  - The simple counter can be configured as an event counter, pulse accumulator, or an interval timer

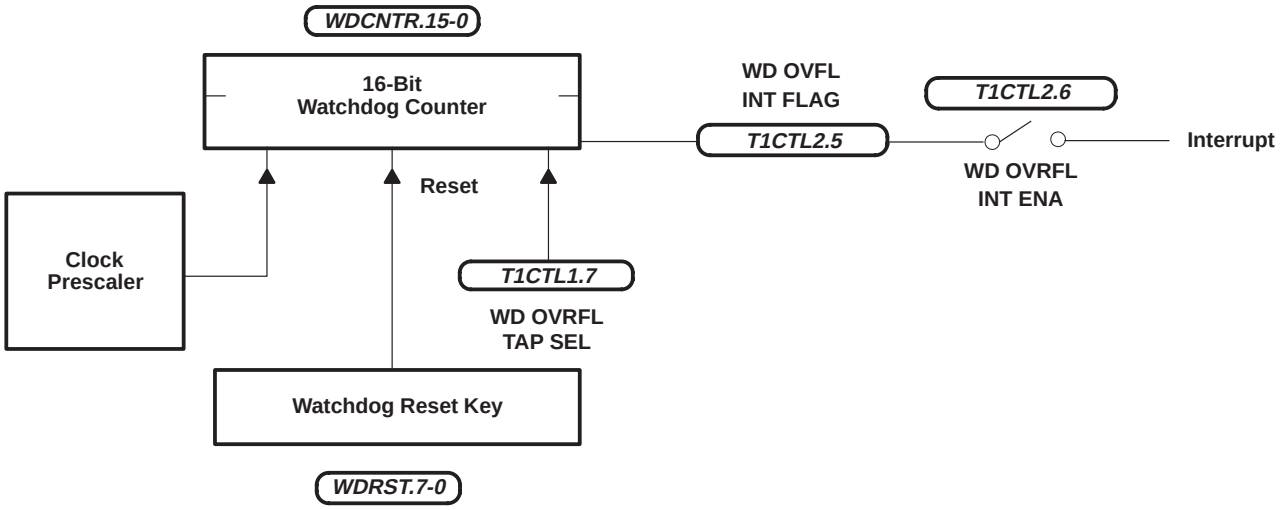


Figure 10. Simple Counter

timer 2A module

The 16-bit general-purpose timer 2A (T2A) module is composed of a 16-bit resettable counter, 16-bit compare register with associated compare logic, 16-bit capture register, and a 16-bit register that functions as a capture register in one mode and as a compare register in the other mode. The T2A module adds an additional timer that provides an event count, input capture, and compare functions. The T2A module includes three external device pins that can be dedicated as timer functions or used as general-purpose I/O pins. The T2A module is shown in Figure 11.

timer 2A module (continued)

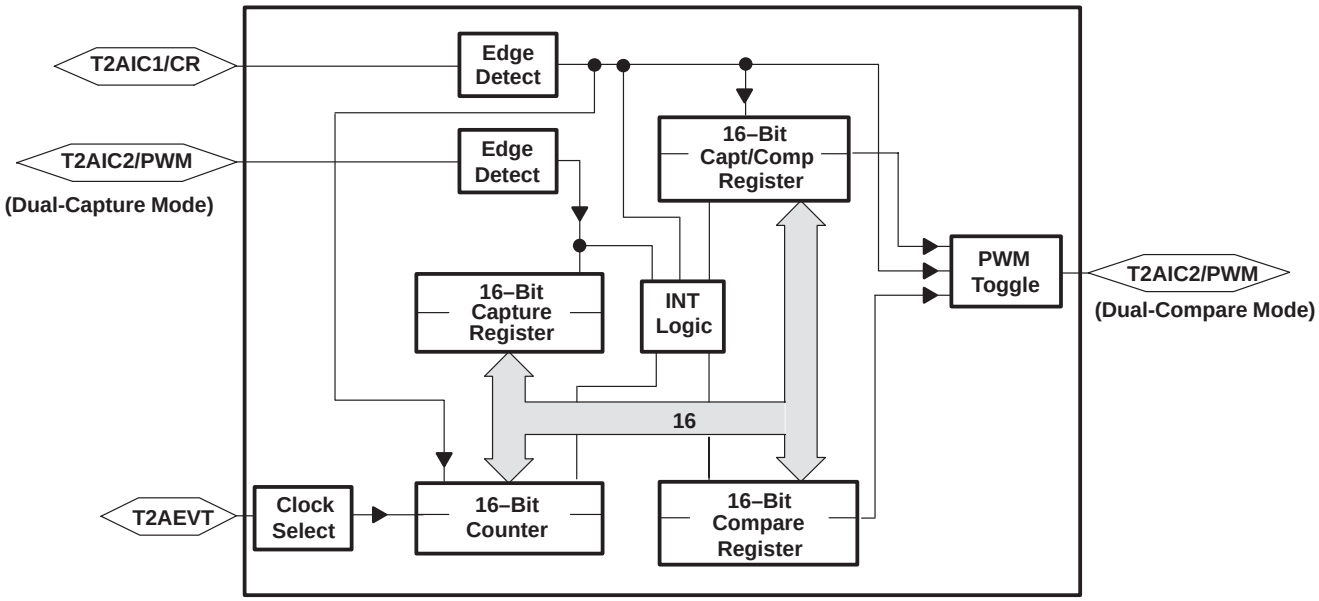


Figure 11. Timer 2A Block Diagram

The T2A module features include the following:

- Three T2A I/O pins:
  - T2AIC1/CR: T2A input-capture 1/counter-reset input pin, or general-purpose bidirectional I/O pin
  - T2AIC2/PWM: T2A input-capture 2/pulse-width-modulation (PWM) output pin, or general-purpose bidirectional I/O pin
  - T2AEVT: Timer 2A event-input pin, or general-purpose bidirectional I/O pin
- Two operational modes:
  - Dual-compare mode: Provides PWM signal
  - Dual-capture mode: Provides input-capture pin
- One 16-bit general-purpose resettable counter
- One 16-bit compare register with associated compare logic
- One 16-bit capture register with associated capture logic
- One 16-bit capture/compare register, which, depending on the mode of operation, operates as either a capture or compare register
- T2A clock sources can be any of the following:
  - System clock
  - No clock (the counter is stopped)
  - External clock synchronized to the system clock (event counter)
  - System clock while external input is high (pulse accumulation)

timer 2A module (continued)

- Selectable edge-detection circuitry that, depending on the mode of operation, senses active transitions on the input capture pins (T2AIC1/CR)
- Interrupts that can be generated on the occurrence of:
  - A compare equal to dedicated compare register
  - A compare equal to capture-compare register
  - A counter overflow
  - An external edge 1 detection
  - An external edge 2 detection
- Fourteen T2A module-control registers: Located in the PF frame beginning at address P060

The T2A module-control registers are illustrated in Table 19.

Table 19. Timer 2A Module Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Modes: Dual-Compare and Dual-Capture								
P060	Bit 15	T2A Counter MSbyte						Bit 8	T2ACNTR
P061	Bit 7	T2A Counter LSbyte						Bit 0	
P062	Bit 15	Compare Register MSbyte						Bit 8	T2AC
P063	Bit 7	Compare Register LSbyte						Bit 0	
P064	Bit 15	Capture/Compare Register MSbyte						Bit 8	T2ACC
P065	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P066	Bit 15	Capture Register 2 MSbyte						Bit 8	T2AIC
P067	Bit 7	Capture Register 2 LSbyte						Bit 0	
P06A	—	—	—	T2A OVRFL INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
	Mode: Dual-Compare								
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
	Mode: Dual-Capture								
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
	Modes: Dual-Compare and Dual-Capture								
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	**T2A STEST**	**T2A PRIORITY**	—	—	—	—	—	—	T2APRI

timer 2A module (continued)

The T2A dual-compare mode block diagram is illustrated in Figure 12. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

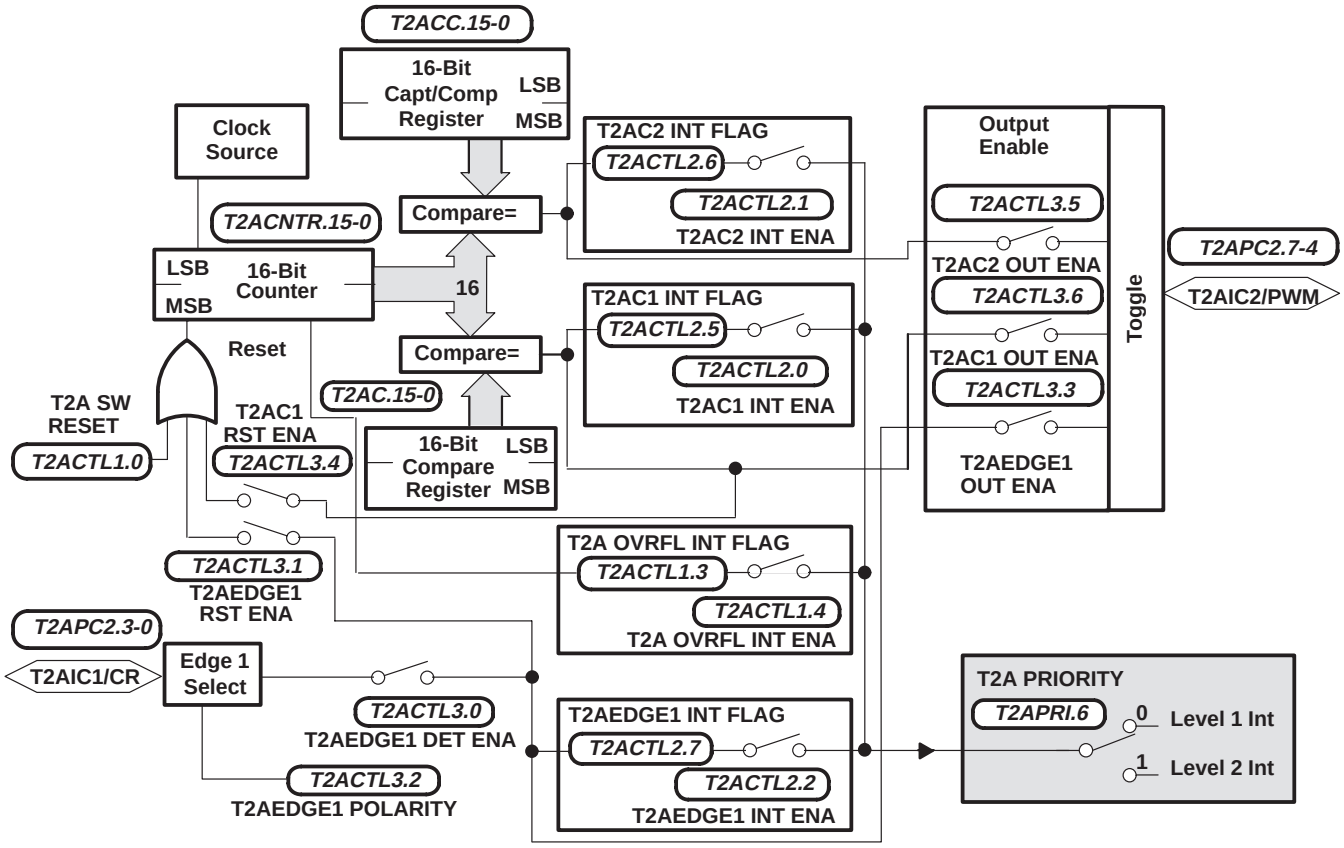


Figure 12. Dual-Compare Mode

timer 2A module (continued)

The T2A dual-capture mode block diagram is illustrated in Figure 13. The annotations on the diagram identify the register and the bit(s) in the peripheral frame. For example, the actual address of T2ACTL2.0 is 106Bh, bit 0, in the T2ACTL2 register.

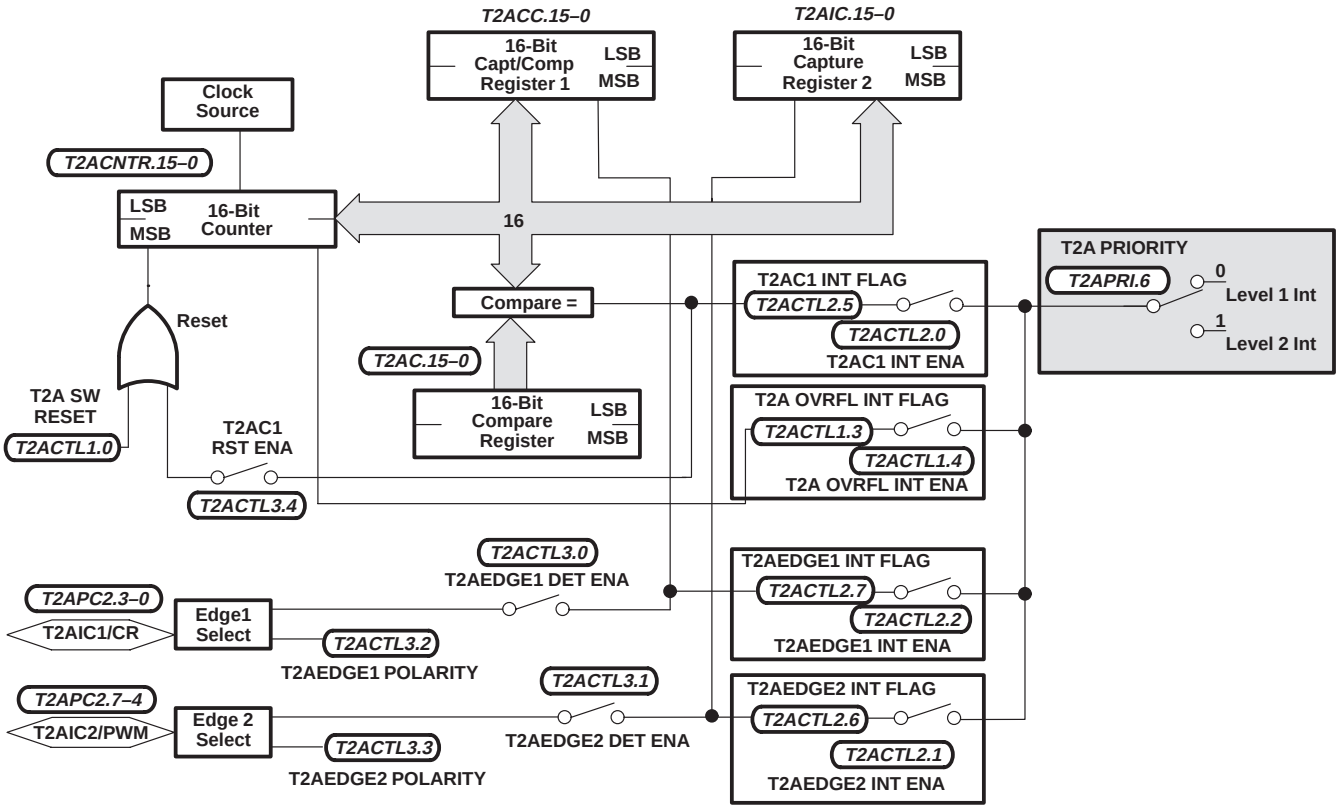


Figure 13. Dual-Capture Mode

serial peripheral interface (SPI) module

The SPI is a high-speed, synchronous, serial I/O port that allows a serial bit stream of programmed length (1 to 8 bits) to be shifted into, and out of, the device at a programmable bit-transfer rate.The SPI is used normally for communications between the microcontroller and external peripherals or another microcontroller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and analog-to-digital converters. The master/slave operation of the SPI supports multi-device communications. The SPI module features include the following:

- Three external pins:
  - SPISOMI: SPI slave output/master input pin or general purpose bidirectional I/O pin
  - SPISIMO: SPI slave input/master output pin or general purpose bidirectional I/O pin
  - SPICLK: SPI serial clock pin or general purpose bidirectional I/O pin
- Two operational modes: master and slave
- Baud rate: Eight different programmable rates
  - Maximum baud rate in master mode: 2.5M bps at 5-MHz SYSCLK

$$\text{SPI BAUD RATE} = \frac{\text{SYSCLK}}{2 \times 2^{b}}$$

  - Maximum baud rate in slave mode: 625K bps at 5-MHz SYSCLK.

    For maximum slave SPI BAUD RATE < SYSCLK/8

  where b = bit rate in SPICCR.5-3 (range 0–7)
- Data word format: one to eight data bits
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt driven or polled algorithms.
- Seven SPI module control registers located in control register frame beginning at address P030h

serial peripheral interface (SPI) module (continued)

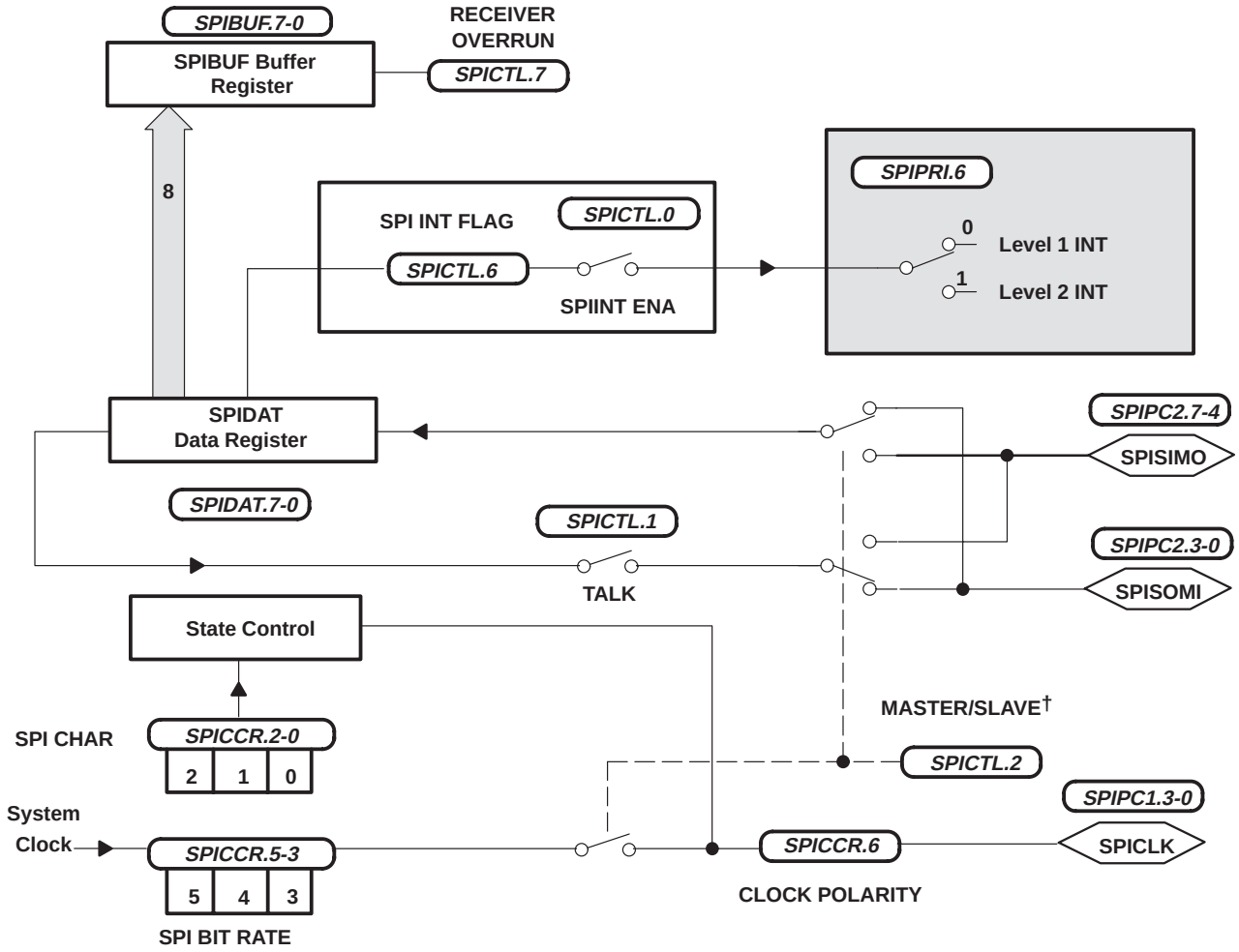
The SPI module control registers are illustrated in Table 20.

Table 20. SPI Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/ SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	**SPI STEST**	**SPI PRIORITY**	**SPI ESPEN**	—	—	—	—	—	SPIPRI

serial peripheral interface (SPI) module (continued)

The SPI block diagram is illustrated in Figure 14.



† The diagram is shown in slave mode.

Figure 14. SPI Block Diagram

serial communications interface 1 (SCI1) module

The TMS370x5x devices include a serial communications interface (SCI1) module. The SCI1 module supports digital communications between the TMS370 devices and other asynchronous peripherals and uses the standard non-return-zero format (NRZ) format. The SCI1's receiver and transmitter are double buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full duplex mode. To ensure data integrity, the SCI1 checks received data for break detection, parity, overrun, and framing errors. The speed of bit rate (baud) is programmable to over 65,000 different speeds through a 16-bit baud-select register.

serial communications interface 1 (SCI1) module (continued)

Features of the SCI1 module include:

- Three external pins:
  - SCITXD: SCI transmit output pin or general-purpose bidirectional I/O pin
  - SCIRXD: SCI receive input pin or general-purpose bidirectional I/O pin
  - SCICLK: SCI bidirectional serial clock pin, or general-purpose bidirectional I/O pin
- Two communications modes: asynchronous and isosynchronous†
- Baud rate: 64K different programmable rates
  - Asynchronous mode: 3 bps to 156K bps at 5-MHz SYSCLK

$$\text{ASYNCHRONOUS BAUD} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 32}$$

  - Isosynchronous mode: 39 bps to 2.5M bps at 5-MHz SYSCLK

$$\text{ISOSYNCHRONOUS BAUD} = \frac{\text{SYSCLK}}{(\text{BAUD REG} + 1) \times 2}$$

- Data-word format
  - One start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: Idle-line and address bit
- Half or full-duplex operation
- Double-buffered receive and transmit functions
- Interrupt driven or polled algorithms with status flags accomplish transmitter (TX) and receiver (RX) operations.
  - Transmitter: TXRDY flag (transmitter buffer register is ready to receive another character) and TX EMPTY flag (transmitter shift register is empty)
  - Receiver: RXRDY flag (receive buffer register ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR monitoring four interrupt conditions
  - Separate enable bits for transmitter and receiver interrupts
  - NRZ (non return-to-zero) format
- Eleven SCI1 module control registers are located in control register frame beginning at address P050h.

† Isosynchronous = Isochronous

serial communications interface 1 (SCI1) module (continued)

The SCI1 module control registers are illustrated in Table 21.

Table 21. SCI1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	**SCI STEST**	**SCITX PRIORITY**	**SCIRX PRIORITY**	**SCI ESPEN**	—	—	—	—	SCIPRI

The SCI1 module block diagram is illustrated in Figure 15.

serial communications interface 1 (SCI1) module (continued)

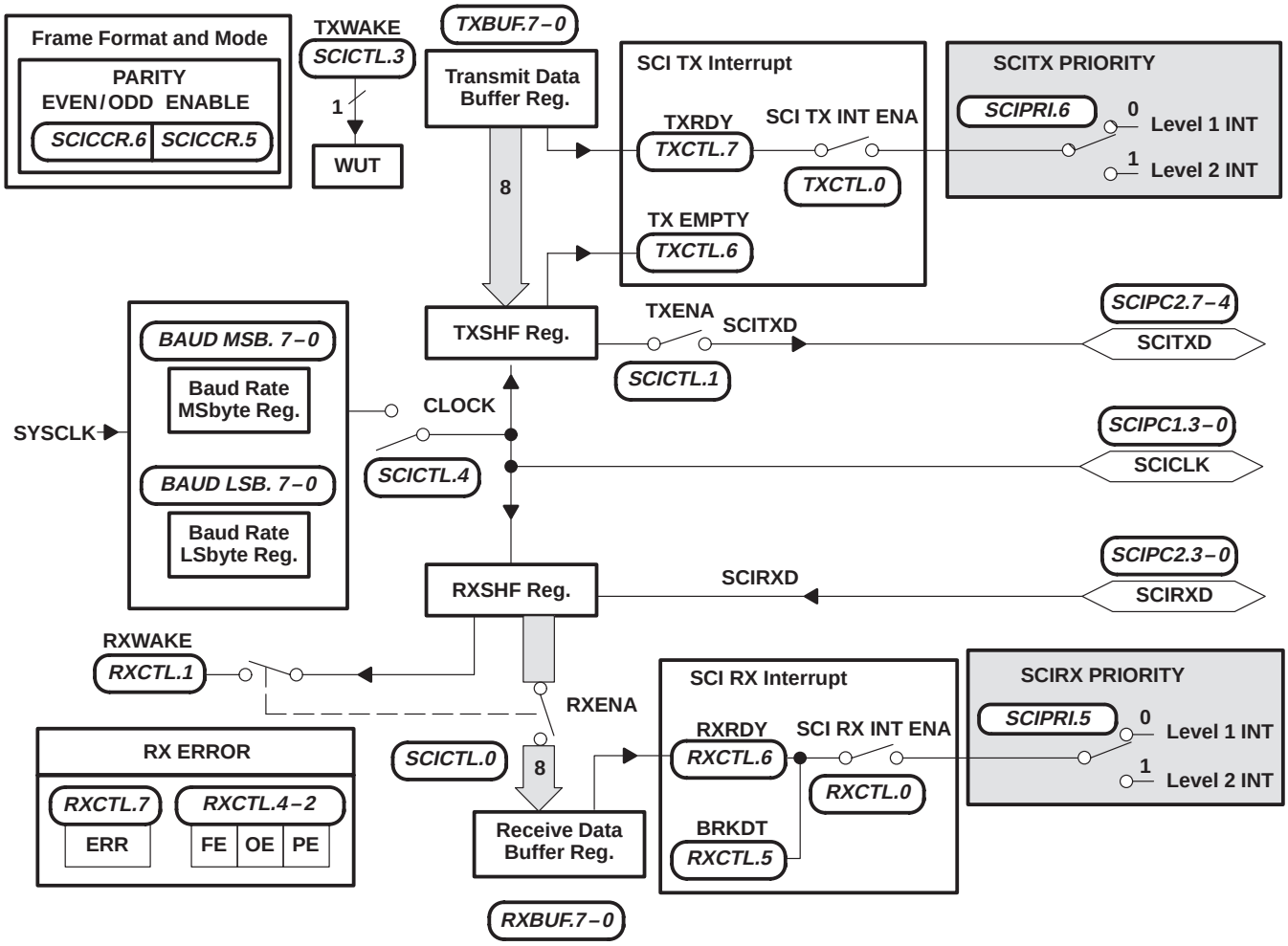


Figure 15. SCI1 Block Diagram

analog-to-digital converter 1 (ADC1) module

The analog-to-digital converter 1 (ADC1) module is an 8-bit, successive approximation converter with internal sample-and-hold circuitry. The module has eight multiplexed analog input channels that allow the processor to convert the voltage levels from up to eight different sources. The ADC1 module features include the following:

- Minimum conversion time: 32.8 µs at 5-MHz SYSCLK
- Ten external pins:
  - Eight analog input channels (AN0–AN7), any of which can be software configured as digital inputs (E0–E7) if not needed as analog channels
  - AN1–AN7 can also be configured as positive-input voltage reference.
  - V_{CC3}: A/D module high-voltage reference input
  - V_{SS3}: A/D module low-voltage reference input

analog-to-digital converter 1 (ADC1) module (continued)

- The ADDATA register, which contains the digital result of the last ADC1 conversion
- ADC1 operations can be accomplished through either interrupt driven or polled algorithms.
- Six ADC1 module control registers are located in the control-register frame beginning at address 1070h.

The ADC1 module control registers are illustrated in Table 22.

Table 22. ADC1 Module Control Register Memory Map

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	**AD STEST**	**AD PRIORITY**	**AD ESPEN**	—	—	—	—	—	ADPRI

analog-to-digital converter 1 (ADC1) module (continued)

The ADC1 module block diagram is illustrated in Figure 16.

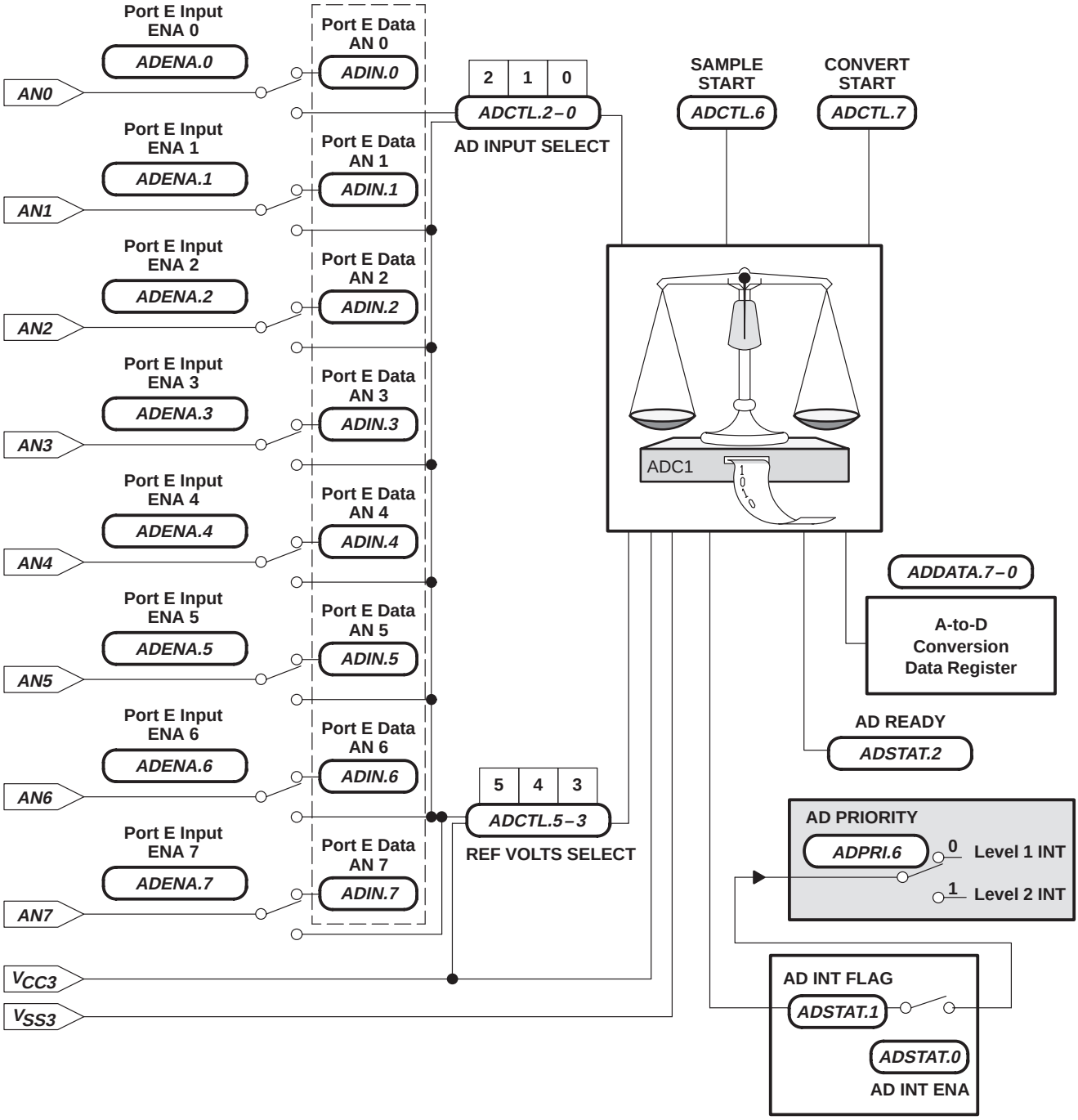


Figure 16. ADC1 Block Diagram

instruction set overview

Table 23 provides an opcode-to-instruction cross-reference of all 73 instructions and 274 opcodes of the ‘370Cx5x instruction set. The numbers at the top of this table represent the most significant nibble of the opcode while the numbers at the left side of the table represent the least significant nibble. The instruction of these two opcode nibbles contains the mnemonic, operands, and byte/cycle particular to that opcode.

For example, the opcode B5h points to the CLR A instruction. This instruction contains one byte and executes in eight SYSCLK cycles.

Table 23. TMS370 Family Opcode/Instruction Map†

MSN

LSN	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	JMP #ra 2/7							INCW #ra,Rd 3/11	MOV Ps,A 2/8			CLRC / TST A 1/9	MOV A,B 1/9	MOV A,Rd 2/7	TRAP 15 1/14	LDST n 2/6
1	JN ra 2/5		MOV A,Pd 2/8			MOV B,Pd 2/8		MOV Rs,Pd 3/10		MOV Ps,B 2/7				MOV B,Rd 2/7	TRAP 14 1/14	MOV #ra[SP],A 2/7
2	JZ ra 2/5	MOV Rs,A 2/7	MOV #n,A 2/6	MOV Rs,B 2/7	MOV Rs,Rd 3/9	MOV #n,B 2/6	MOV B,A 1/8	MOV #n,Rd 3/8			MOV Ps,Rd 3/10	DEC A 1/8	DEC B 1/8	DEC Rd 2/6	TRAP 13 1/14	MOV A,*ra[SP] 2/7
3	JC ra 2/5	AND Rs,A 2/7	AND #n,A 2/6	AND Rs,B 2/7	AND Rs,Rd 3/9	AND #n,B 2/6	AND B,A 1/8	AND #n,Rd 3/8	AND A,Pd 2/9	AND B,Pd 2/9	AND #n,Pd 3/10	INC A 1/8	INC B 1/8	INC Rd 2/6	TRAP 12 1/14	CMP *n[SP],A 2/8
4	JP ra 2/5	OR Rs,A 2/7	OR #n,A 2/6	OR Rs,B 2/7	OR Rs,Rd 3/9	OR #n,B 2/6	OR B,A 1/8	OR #n,Rd 3/8	OR A,Pd 2/9	OR B,Pd 2/9	OR #n,Pd 3/10	INV A 1/8	INV B 1/8	INV Rd 2/6	TRAP 11 1/14	extend inst,2 opcodes
5	JPZ ra 2/5	XOR Rs,A 2/7	XOR #n,A 2/6	XOR Rs,B 2/7	XOR Rs,Rd 3/9	XOR #n,B 2/6	XOR B,A 1/8	XOR #n,Rd 3/8	XOR A,Pd 2/9	XOR B,Pd 2/9	XOR #n,Pd 3/10	CLR A 1/8	CLR B 1/8	CLR Rn 2/6	TRAP 10 1/14	
6	JNZ ra 2/5	BTJO Rs,A,ra 3/9	BTJO #n,A,ra 3/8	BTJO Rs,B,ra 3/9	BTJO Rs,Rd,ra 4/11	BTJO #n,B,ra 3/8	BTJO B,A,ra 2/10	BTJO #n,Rd,ra 4/10	BTJO A,Pd,ra 3/11	BTJO B,Pd,ra 3/10	BTJO #n,Pd,ra 4/11	XCHB A 1/10	XCHB A / TST B 1/10	XCHB Rn 2/8	TRAP 9 1/14	IDLE 1/6
7	JNC ra 2/5	BTJZ Rs.,A,ra 3/9	BTJZ #n,A,ra 3/8	BTJZ Rs,B,ra 3/9	BTJZ Rs,Rd,ra 4/11	BTJZ #n,B,ra 3/8	BTJZ B,A,ra 2/10	BTJZ #n,Rd,ra 4/10	BTJZ A,Pd,ra 3/10	BTJZ B,Pd,ra 3/10	BTJZ #n,Pd,ra 4/11	SWAP A 1/11	SWAP B 1/11	SWAP Rn 2/9	TRAP 8 1/14	MOV #n,Pd 3/10
8	JV ra 2/5	ADD Rs,A 2/7	ADD #n,A 2/6	ADD Rs,B 2/7	ADD Rs,Rd 3/9	ADD #n,B 2/6	ADD B,A 1/8	ADD #n,Rd 3/8	MOVW #16,Rd 4/13	MOVW Rs,Rd 3/12	MOVW #16[B],Rpd 4/15	PUSH A 1/9	PUSH B 1/9	PUSH Rd 2/7	TRAP 7 1/14	SETC 1/7
9	JL ra 2/5	ADC Rs,A 2/7	ADC #n,A 2/6	ADC Rs,B 2/7	ADC Rs,Rd 3/9	ADC #n,B 2/6	ADC B,A 1/8	ADC #n,Rd 3/8	JMPL lab 3/9	JMPL *Rp 2/8	JMPL *lab[B] 3/11	POP A 1/9	POP B 1/9	POP Rd 2/7	TRAP 6 1/14	RTS 1/9
A	JLE ra 2/5	SUB Rs,A 2/7	SUB #n,A 2/6	SUB Rs,B 2/7	SUB Rs,Rd 3/9	SUB #n,B 2/6	SUB B,A 1/8	SUB #n,Rd 3/8	MOV & lab,A 3/10	MOV *Rp,A 2/9	MOV *lab[B],A 3/12	DJNZ A,#ra 2/10	DJNZ B,#ra 2/10	DJNZ Rd,#ra 3/8	TRAP 5 1/14	RTI 1/12
B	JHS ra 2/5	SBB Rs,A 2/7	SBB #n,A 2/6	SBB Rs,B 2/7	SBB Rs,Rd 3/9	SBB #n,B 2/6	SBB B,A 1/8	SBB #n,Rd 3/8	MOV A, & lab 3/10	MOV A, *Rp 2/9	MOV A,*lab[B] 3/12	COMPL A 1/8	COMPL B 1/8	COMPL Rd 2/6	TRAP 4 1/14	PUSH ST 1/8

† All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

Table 23. TMS370 Family Opcode/Instruction Map† (Continued)

MSN

LSN	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C	JNV ra 2/5	MPY Rs,A 2/46	MPY #n,A 2/45	MPY Rs,B 2/46	MPY Rs,Rd 3/48	MPY #n,B 2/45	MPY B,A 1/47	MPY #n,Rs 3/47	BR lab 3/9	BR *Rp 2/8	BR *lab[B] 3/11	RR A 1/8	RR B 1/8	RR Rd 2/6	TRAP 3 1/14	POP ST 1/8
D	JGE ra 2/5	CMP Rs,A 2/7	CMP #n,A 2/6	CMP Rs,B 2/7	CMP Rs,Rd 3/9	CMP #n,B 2/6	CMP B,A 1/8	CMP #n,Rd 3/8	CMP & lab,A 3/11	CMP *Rp,A 2/10	CMP *lab[B],A 3/13	RRC A 1/8	RRC B 1/8	RRC Rd 2/6	TRAP 2 1/14	LDSP 1/7
E	JG ra 2/5	DAC Rs,A 2/9	DAC #n,A 2/8	DAC Rs,B 2/9	DAC Rs,Rd 3/11	DAC #n,B 2/8	DAC B,A 1/10	DAC #n,Rd 3/10	CALL lab 3/13	CALL *Rp 2/12	CALL *lab[B] 3/15	RL A 1/8	RL B 1/8	RL Rd 2/6	TRAP 1 1/14	STSP 1/8
F	JLO ra 2/5	DSB Rs,A 2/9	DSB #n,A 2/8	DSB Rs,B 2/9	DSB Rs,Rd 3/11	DSB #n,B 2/8	DSB B,A 1/10	DSB #n,Rd 3/10	CALLR lab 3/15	CALLR *Rp 2/14	CALLR *lab[B] 3/17	RLC A 1/8	RLC B 1/8	RLC Rd 2/6	TRAP 0 1/14	NOP 1/7

Second byte of two-byte instructions (F4xx):			
F4	8	MOVW *n[Rn] 4/15	DIV Rn.A 3/14-63
F4	9	JMPL *n[Rn] 4/16	
F4	A	MOV *n[Rn],A 4/17	
F4	B	MOV A,*n[Rn] 4/16	
F4	C	BR *n[Rn] 4/16	
F4	D	CMP *n[Rn],A 4/18	
F4	E	CALL *n[Rn] 4/20	
F4	F	CALLR *n[Rn] 4/22	

Legend:
* = Indirect addressing operand prefix
& = Direct addressing operand prefix
# = immediate operand
#16 = immediate 16-bit number
lab = 16-label
n = immediate 8-bit number
Pd = Peripheral register containing destination type
Pn = Peripheral register
Ps = Peripheral register containing source byte
ra = Relative address
Rd = Register containing destination type
Rn = Register file
Rp = Register pair
Rpd = Destination register pair
Rps = Source Register pair
Rs = Register containing source byte

† All conditional jumps (opcodes 01–0F), BTJO, BTJZ, and DJNZ instructions use two additional cycles if the branch is taken. The BTJO, BTJZ, and DJNZ instructions have a relative address as the last operand.

development system support

The TMS370 family development support tools include an assembler, a C compiler, a linker, an in-circuit emulator (XDS/22), CDT, and an EEPROM/UVEPROM programmer.

- Assembler/linker (Part No. TMDS3740850–02 for PC)
  - Includes extensive macro capability
  - Features high-speed operation
  - Includes format conversion utilities for popular formats
- ANSI C-Compiler (Part No. TMDS3740855–02 for PC, Part No. TMDS3740555–09 for HP700™, Sun-3™ or Sun-4™)
  - Generates assembly code for the TMS370 that can be inspected easily
  - Improves code execution speed and reduces code size with optional optimizer pass
  - Enables direct reference of the TMS370's port registers by using a naming convention
  - Provides flexibility in specifying the storage for data objects
  - Interfaces C functions and assembly functions easily
  - Includes assembler and linker
- CDT370 (compact development tool) real-time in-circuit emulation
  - Base (Part Number EDSCDT370 – for PC, requires cable)
    - Cable for 68-pin PLCC (Part No. EDSTRG68PLCC)
    - Cable for 64-pin SDIP (Part No. EDSTRG64SDIL)
  - Provides EEPROM and EPROM programming support
  - Allows inspection and modification of memory locations
  - Allows uploading/downloading of program and data memory
  - Provides capability to execute programs and software routines
  - Includes 1024 samples trace buffer
  - Includes single-step executable instructions
  - Allows use of software breakpoints to halt program execution at selected address
- XDS/22 (extended development support) in-circuit emulator
  - Base (Part Number TMDS3762210 for PC, requires cable)
  - Cable for 68-pin PLCC/64-Pin SDIP (Part No. TMDS3788868)
  - Contains all of the features of the CDT370 described above but does not have the capability to program the data EEPROM and program EPROM
  - Contains sophisticated breakpoint trace and timing hardware that provides up to 2047 qualified trace samples with symbolic disassembly
  - Allows breakpoints to be qualified by address and/or data on any type of memory acquisition. Up to four levels of events can be combined to cause a breakpoint
  - Provides timers for analyzing total and average time in routines

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development system support (continued)

- – Contains an eight-line logic probe for adding visibility of external signals to the breakpoint qualifier and for tracing display

- Microcontroller programmer
  - – Base (Part No. TMDS3760500A – for PC, requires programmer head)
    - – Single unit head for 68-pin PLCC (Part No. TMDS3780510A)
    - – Single unit head for 64-pin SDIP (Part No. TMDS3780511A)
  - – Personal computer-based, window/function-key oriented user interface for ease of use and rapid learning environment
- Design kit (Part No. TMDS3770110 – for PC)
  - – Includes TMS370 Application Board and TMS370 Assembler diskette and documentation.
  - – Supports quick evaluation of TMS370 functionality
  - – Provides capability to upload and download code
  - – Provides capability to execute programs and software routines, and to single-step executable instructions
  - – Allows software breakpoints to halt program execution at selected addresses
  - – Includes wire-wrap prototype area
  - – Includes reverse assembler
- Starter Kit (Part No. TMDS37000 – For PC)
  - – Includes TMS370 Assembler diskette and documentation
  - – Includes TMS370 Simulator
  - – Includes programming adapter board and programming software
  - – Does not include – (to be supplied by the user):
    - – + 5 V power supply
    - – ZIF sockets
    - – 9-pin RS232 cable

device numbering conventions

Figure 17 illustrates the numbering and symbol nomenclature for the TMS370Cx5x family.

TMS 370 C 7 5 2 A FN T

Prefix:
- **TMS = Standard prefix for fully qualified devices**
- **SE = System evaluator (window EPROM) that is used for prototyping purpose.**

Family:
- **370 = TMS370 8-Bit Microcontroller Family**

Technology:
- **C = CMOS**

Program Memory Types:
- **0 = Mask ROM**
- **1 = ROM-less, No Data EEPROM**
- **2 = ROM-less**
- **3 = Mask ROM, No Data EEPROM**
- **4 = ROM memory with security**
- **7 = EPROM**

Device Type:
- **5 = ’x5x device containing the following modules:**
  - **– Timer 1**
  - **– Timer 2A**
  - **– Serial Peripheral Interface**
  - **– Serial Communications Interface 1**
  - **– Analog-to-Digital Converter 1**

Memory Size:
- **0 = 4K bytes**
- **2 = 8K bytes**
- **3 = 12K bytes**
- **6 = 16K bytes**
- **8 = 32K Bytes**
- **9 = 48K Bytes**

Temperature Ranges:
- **A = –40°C to 85°C**
- **L = 0°C to 70°C**
- **T = –40°C to 105°C**

Packages:
- **FN = Plastic Leaded Chip Carrier**
- **FZ = Ceramic Leaded Chip Carrier**
- **NM = Plastic Shrink Dual-In-Line**
- **JN = Ceramic Shrink Dual-in-Line**

ROM and EPROM Option:
- **A = For ROM device, the watchdog timer can be configured as one of the three different mask options:**
  - **– A standard watchdog**
  - **– A hard watchdog**
  - **– A simple watchdog**

  The clock can be either:
  - **– Divide-by-4 clock**
  - **– Divide-by-1 (PLL) clock**

  The low-power modes can be either:
  - **– Enabled**
  - **– Disabled**
- **A = For ROM-less device, a standard watchdog, a divide-by-4 clock, and low-power modes are enabled.**
- **A = For EPROM device, a standard watchdog, a divide-by-4 clock, and low-power modes are enabled.**
- **B = For EPROM device, a hard watchdog, a divide-by-1 (PLL) clock, and low-power modes are enabled.**

Figure 17. TMS370Cx5x Family Nomenclature

device part numbers

Table 24 provides a list of all the ‘x5x devices available. The device part number nomenclature is designed to assist ordering. Upon ordering, the customer must specify not only the device part number but also the clock and watchdog timer options desired. Remember that each device can have only one of the three possible watchdog timer options and one of the two clock options. The options to be specified pertain solely to orders involving ROM devices.

Table 24. Device Part Numbers

DEVICE PART NUMBERS FOR 68 PINS	DEVICE PART NUMBERS FOR 64 PINS	DEVICE PART NUMBERS FOR 68 PINS	DEVICE PART NUMBERS FOR 64 PINS
TMS370C050AFNA TMS370C050AFNL TMS370C050AFNT	TMS370C050ANMA TMS370C050ANML TMS370C050ANMT	TMS370C356AFNA TMS370C356AFNL TMS370C356AFNT	TMS370C356ANMA TMS370C356ANML TMS370C356ANMT
TMS370C150AFNT	—	TMS370C456AFNA TMS370C456AFNL TMS370C456AFNT	—
TMS370C250AFNT	—	TMS370C756AFNT	TMS370C756ANMT
TMS370C350AFNA TMS370C350AFNL TMS370C350AFNT	TMS370C350ANMA TMS370C350ANML TMS370C350ANMT	TMS370C058AFNA TMS370C058AFNL TMS370C058AFNT	TMS370C058ANMA TMS370C058ANML TMS370C058ANMT
TMS370C052AFNA TMS370C052AFNL TMS370C052AFNT	TMS370C052ANMA TMS370C052ANML TMS370C052ANMT	TMS370C358AFNA TMS370C358AFNL TMS370C358AFNT	TMS370C358ANMA TMS370C358ANML TMS370C358ANMT
TMS370C352AFNA TMS370C352AFNL TMS370C352AFNT	TMS370C352ANMA TMS370C352ANML TMS370C352ANMT	TMS370C758AFNT	TMS370C758ANMT
TMS370C452AFNA TMS370C452AFNL TMS370C452AFNT	—	TMS370C758BFNT	TMS370C758BNMT
TMS370C353AFNA TMS370C353AFNL TMS370C353AFNT	—	TMS370C059AFNA† TMS370C059AFNL† TMS370C059AFNT†	—
TMS370C056AFNA TMS370C056AFNL TMS370C056AFNT	TMS370C056ANMA TMS370C056ANML TMS370C056ANMT	TMS370C759AFNT†	—
TMS370C156AFNT	—	SE370C756AFZT‡ SE370C758AFZT‡ SE370C758BFZT‡ SE370C759AFZT†‡	SE370C756AJNT‡ SE370C758AJNT‡ SE370C758BJNT‡
TMS370C256AFNT	—		

† Only operate up to 3 MHz SYSCLK
‡ System evaluators are for use only in prototype environment, and their reliability has not been characterized.

new code release form

Figure 18 shows a sample of the new code release form.

NEW CODE RELEASE FORM
TEXAS INSTRUMENTS
TMS370 MICROCONTROLLER PRODUCTS

DATE: _____

To release a new customer algorithm to TI incorporated into a TMS370 family microcontroller, complete this form and submit with the following information:

1. A ROM description in object form on Floppy Disk, Modem XFR, or EPROM (Verification file will be returned via same media)
2. An attached specification if not using TI standard specification as incorporated in TI's applicable device data book.

Company Name: _____
Street Address: _____
Street Address: _____
City: _____ State _____ Zip _____

Customer Part Number: _____
Customer Application: _____

TMS370 Device: _____

TI Customer ROM Number: _____
(provided by Texas Instruments)

OSCILLATOR FREQUENCY

	MIN	TYP	MAX
[] External Drive (CLKIN)	_____	_____	_____
[] Crystal	_____	_____	_____
[] Ceramic Resonator	_____	_____	_____

[] Supply Voltage MIN: _____ MAX: _____
(std range: 4.5V to 5.5V)

TEMPERATURE RANGE
[] 'L': 0° to 70°C (standard)
[] 'A': –40° to 85°C
[] 'T': –40° to 105°C

SYMBOLIZATION
[] TI standard symbolization
[] TI standard w/customer part number
[] Customer symbolization
(per attached spec, subject to approval)

Contact Mr./Ms.: _____
Phone: (_____)_____ Ext.: _____

Customer Purchase Order Number: _____

Customer Print Number *Yes:____ # _____
No: ____ (Std. spec to be followed)
*If Yes: Customer must provide "print" to TI w/NCRF for approval before ROM code processing starts.

CONTACT OPTIONS FOR THE 'A' VERSION TMS370 MICROCONTROLLERS

Low Power Modes	Watchdog counter	Clock Type
[] Enabled	[] Standard	[] Standard (/4)
[] Disabled	[] Hard Enabled	[] PLL (/1)
	[] Simple Counter	

NOTE:
Non 'A' version ROM devices of the TMS370 microcontrollers will have the "Low-power modes Enabled", "Divide-by-4" Clock, and "Standard" Watchdog options. See the *TMS370 Family User's Guide* (literature number SPNU127) or the *TMS370 Family Data Manual* (literature number SPNS014B).

PACKAGE TYPE
[] 'N' 28-pin PDIP
[] "FN" 28-pin PLCC
[] "N" 40-pin PDIP
[] "NJ" 40-pin PSDIP (formerly known as N2)
[] "FN" 44-pin PLCC
[] "FN" 68-pin PLCC
[] "NM" 64-pin PSDIP

BUS EXPANSION
[] YES [] NO

NON-STANDARD SPECIFICATIONS:
ALL NON-STANDARDS SPECIFICATIONS MUST BE APPROVED BY THE TI ENGINEERING STAFF: If the customer requires expedited production material (i.e., product which must be started in process prior to prototype approval and full production release) and non-standard spec issues are not resolved to the satisfaction of both the customer and TI in time for a scheduled shipment, the specification parameters in question will be processed/tested to the standard TI spec. Any such devices which are shipped without conformance to a mutually approved spec, will be identified by a 'P' in the symbolization preceding the TI part number.

RELEASE AUTHORIZATION:
This document, including any referenced attachments, is and will be the controlling document for all orders placed for this TI custom device. Any changes must be in writing and mutually agreed to by both the customer and TI. The prototype cycletime commences when this document is signed off and the verification code is approved by the customer.

1. Customer: _____ Date: _____

2. TI: Field Sales: _____
Marketing: _____
Prod. Eng.: _____
Proto. Release: _____

Figure 18. Sample New Code Release Form

Table 25 is a listing of all the peripheral file frames using the ’Cx5x (provided for a quick reference).

Table 25. Peripheral File Frame Compilation

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	SYSTEM CONFIGURATION REGISTERS								
P010	COLD START	**OSC POWER**	**PF AUTO WAIT**	OSC FLT FLAG	MC PIN WPO	MC PIN DATA	—	µP/µC MODE	SCCR0
P011		—	—	**AUTOWAIT DISABLE**	—	**MEMORY DISABLE**	—	—	SCCR1
P012	**HALT/ STANDBY**	**PWRDWN/ IDLE**	—	**BUS STEST**	**CPU STEST**	—	**INT1 NMI**	**PRIVILEGE DISABLE**	SCCR2
P013	Reserved								
P014	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLH
P015 to P016	Reserved								
P017	INT1 FLAG	INT1 PIN DATA	—	—	—	INT1 POLARITY	INT1 PRIORITY	INT1 ENABLE	INT1
P018	INT2 FLAG	INT2 PIN DATA	—	INT2 DATA DIR	INT2 DATA OUT	INT2 POLARITY	INT2 PRIORITY	INT2 ENABLE	INT2
P019	INT3 FLAG	INT3 PIN DATA	—	INT3 DATA DIR	INT3 DATA OUT	INT3 POLARITY	INT3 PRIORITY	INT3 ENABLE	INT3
P01A	BUSY	—	—	—	—	AP	W1W0	EXE	DEECTL
P01B	Reserved								
P01C	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLM
P01D	Reserved								
P01E	BUSY	VPPS	—	—	—	—	W0	EXE	EPCTLL
	DIGITAL PORT CONTROL REGISTERS								
P01F	Reserved								
P020	Reserved								APORT1
P021	Port A Control Register 2								APORT2
P022	Port A Data								ADATA
P023	Port A Direction								ADIR
P024	Reserved								BPORT1
P025	Port B Control Register 2								BPORT2
P026	Port B Data								BDATA
P027	Port B Direction								BDIR
P028	Reserved								CPORT1
P029	Port C Control Register 2								CPORT2
P02A	Port C Data								CDATA
P02B	Port C Direction								CDIR
P02C	Port D Control Register 1								DPORT1
P02D	Port D Control Register 2†								DPORT2
P02E	Port D Data								DDATA
P02F	Port D Direction								DDIR

† To configure pin D3 as SYSCLK, set port D control register 2 = 08h.

Table 25. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	SPI MODULE CONTROL REGISTER								
P030	SPI SW RESET	CLOCK POLARITY	SPI BIT RATE2	SPI BIT RATE1	SPI BIT RATE0	SPI CHAR2	SPI CHAR1	SPI CHAR0	SPICCR
P031	RECEIVER OVERRUN	SPI INT FLAG	—	—	—	MASTER/ SLAVE	TALK	SPI INT ENA	SPICTL
P032 to P036	Reserved								
P037	RCVD7	RCVD6	RCVD5	RCVD4	RCVD3	RCVD2	RCVD1	RCVD0	SPIBUF
P038	Reserved								
P039	SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0	SPIDAT
P03A to P03C	Reserved								
P03D	—	—	—	—	SPICLK DATA IN	SPICLK DATA OUT	SPICLK FUNCTION	SPICLK DATA DIR	SPIPC1
P03E	SPISIMO DATA IN	SPISIMO DATA OUT	SPISIMO FUNCTION	SPISIMO DATA DIR	SPISOMI DATA IN	SPISOMI DATA OUT	SPISOMI FUNCTION	SPISOMI DATA DIR	SPIPC2
P03F	**SPI STEST**	**SPI PRIORITY**	**SPI ESPEN**	—	—	—	—	—	SPIPRI
	TIMER 1 MODULE REGISTER								
	Modes: Dual-Compare and Capture / Compare								
P040	Bit 15	T1 Counter MSbyte						Bit 8	T1CNTR
P041	Bit 7	T1 Counter LSbyte						Bit 0	
P042	Bit 15	Compare Register MSbyte						Bit 8	T1C
P043	Bit 7	Compare Register LSbyte						Bit 0	
P044	Bit 15	Capture/Compare Register MSbyte						Bit 8	T1CC
P045	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P046	Bit 15	Watchdog Counter MSbyte						Bit 8	WDCNTR
P047	Bit 7	Watchdog Counter LSbyte						Bit 0	
P048	Bit 15	Watchdog Reset Key						Bit 0	WDRST
P049	WD OVRFL TAP SEL†	WD INPUT SELECT2†	WD INPUT SELECT1†	WD INPUT SELECT0†	—	T1 INPUT SELECT2	T1 INPUT SELECT1	T1 INPUT SELECT0	T1CTL1
P04A	WD OVRFL RST ENA†	WD OVRFL INT ENA	WD OVRFL INT FLAG	T1 OVRFL INT ENA	T1 OVRFL INT FLAG	—	—	T1 SW RESET	T1CTL2
	Mode: Dual-Compare								
P04B	T1EDGE INT FLAG	T1C2 INT FLAG	T1C1 INT FLAG	—	—	T1EDGE INT ENA	T1C2 INT ENA	T1C1 INT ENA	T1CTL3
P04C	T1 MODE = 0	T1C1 OUT ENA	T1C2 OUT ENA	T1C1 RST ENA	T1CR OUT ENA	T1EDGE POLARITY	T1CR RST ENA	T1EDGE DET ENA	T1CTL4
	Mode: Capture/Compare								
P04B	T1EDGE INT FLAG	—	T1C1 INT FLAG	—	—	T1EDGE INT ENA	—	T1C1 INT ENA	T1CTL3

† Once the WD OVRFL RST ENA bit is set, these bits cannot be changed until a reset; this applies only to the standard watchdog and to the simple counter. In the hard watchdog, these bits can be modified at any time; the WD INPUT SELECT2 bits are ignored.

Table 25. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Mode: Capture/Compare (Continued)								
P04C	T1 MODE = 1	T1C1 OUT ENA	—	T1C1 RST ENA	—	T1EDGE POLARITY	—	T1EDGE DET ENA	T1CTL4
	Modes: Dual-Compare and Capture / Compare								
P04D	—	—	—	—	T1EVT DATA IN	T1EVT DATA OUT	T1EVT FUNCTION	T1EVT DATA DIR	T1PC1
P04E	T1PWM DATA IN	T1PWM DATA OUT	T1PWM FUNCTION	T1PWM DATA DIR	T1IC/CR DATA IN	T1IC/CR DATA OUT	T1IC/CR FUNCTION	T1IC/CR DATA DIR	T1PC2
P04F	**T1 STEST**	**T1 PRIORITY**	—	—	—	—	—	—	T1PRI
	SCI1 MODULE CONTROL REGISTER								
P050	STOP BITS	EVEN/ODD PARITY	PARITY ENABLE	ASYNC/ ISOSYNC	ADDRESS/ IDLE WUP	SCI CHAR2	SCI CHAR1	SCI CHAR0	SCICCR
P051	—	—	SCI SW RESET	CLOCK	TXWAKE	SLEEP	TXENA	RXENA	SCICTL
P052	BAUDF (MSB)	BAUDE	BAUDD	BAUDC	BAUDB	BAUDA	BAUD9	BAUD8	BAUD MSB
P053	BAUD7	BAUD6	BAUD5	BAUD4	BAUD3	BAUD2	BAUD1	BAUD0 (LSB)	BAUD LSB
P054	TXRDY	TX EMPTY	—	—	—	—	—	SCI TX INT ENA	TXCTL
P055	RX ERROR	RXRDY	BRKDT	FE	OE	PE	RXWAKE	SCI RX INT ENA	RXCTL
P056	Reserved								
P057	RXDT7	RXDT6	RXDT5	RXDT4	RXDT3	RXDT2	RXDT1	RXDT0	RXBUF
P058	Reserved								
P059	TXDT7	TXDT6	TXDT5	TXDT4	TXDT3	TXDT2	TXDT1	TXDT0	TXBUF
P05A P05B P05C	Reserved								
P05D	—	—	—	—	SCICLK DATA IN	SCICLK DATA OUT	SCICLK FUNCTION	SCICLK DATA DIR	SCIPC1
P05E	SCITXD DATA IN	SCITXD DATA OUT	SCITXD FUNCTION	SCITXD DATA DIR	SCIRXD DATA IN	SCIRXD DATA OUT	SCIRXD FUNCTION	SCIRXD DATA DIR	SCIPC2
P05F	**SCI STEST**	**SCITX PRIORITY**	**SCIRX PRIORITY**	**SCI ESPEN**	—	—	—	—	SCIPRI
	T2A MODULE REGISTER								
	Modes: Dual-Compare and Dual-Capture								
P060	Bit 15	T2A Counter MSbyte						Bit 8	T2ACNTR
P061	Bit 7	T2A Counter LSbyte						Bit 0	
P062	Bit 15	Compare Register MSbyte						Bit 8	T2AC
P063	Bit 7	Compare Register LSbyte						Bit 0	
P064	Bit 15	Capture/Compare Register MSbyte						Bit 8	T2ACC
P065	Bit 7	Capture/Compare Register LSbyte						Bit 0	
P066	Bit 15	Capture Register 2 MSbyte						Bit 8	T2AIC
P067	Bit 7	Capture Register 2 LSbyte						Bit 0	

Table 25. Peripheral File Frame Compilation (Continued)

PF	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	REG
	Modes: Dual-Compare and Dual-Capture (Continued)								
P06A	—	—	—	T2A OVRFL-INT ENA	T2A OVRFL INT FLAG	T2A INPUT SELECT1	T2A INPUT SELECT0	T2A SW RESET	T2ACTL1
	Mode: Dual-Compare								
P06B	T2AEDGE1 INT FLAG	T2AC2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AC2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 0	T2AC1 OUT ENA	T2AC2 OUT ENA	T2AC1 RST ENA	T2AEDGE1 OUT ENA	T2AEDGE1 POLARITY	T2AEDGE1 RST ENA	T2AEDGE1 DET ENA	T2ACTL3
	Mode: Dual-Capture								
P06B	T2AEDGE1 INT FLAG	T2AEDGE2 INT FLAG	T2AC1 INT FLAG	—	—	T2AEDGE1 INT ENA	T2AEDGE2 INT ENA	T2AC1 INT ENA	T2ACTL2
P06C	T2A MODE = 1	—	—	T2AC1 RST ENA	T2AEDGE2 POLARITY	T2AEDGE1 POLARITY	T2AEDGE2 DET ENA	T2AEDGE1 DET ENA	T2ACTL3
	Modes: Dual-Compare and Dual-Capture								
P06D	—	—	—	—	T2AEVT DATA IN	T2AEVT DATA OUT	T2AEVT FUNCTION	T2AEVT DATA DIR	T2APC1
P06E	T2AIC2/PWM DATA IN	T2AIC2/PWM DATA OUT	T2AIC2/PWM FUNCTION	T2AIC2/PWM DATA DIR	T2AIC1/CR DATA IN	T2AIC1/CR DATA OUT	T2AIC1/CR FUNCTION	T2AIC1/CR DATA DIR	T2APC2
P06F	**T2A STEST**	**T2A PRIORITY**	—	—	—	—	—	—	T2APRI
	ADC1 MODULE CONTROL REGISTER								
P070	CONVERT START	SAMPLE START	REF VOLT SELECT2	REF VOLT SELECT1	REF VOLT SELECT0	AD INPUT SELECT2	AD INPUT SELECT1	AD INPUT SELECT0	ADCTL
P071	—	—	—	—	—	AD READY	AD INT FLAG	AD INT ENA	ADSTAT
P072	A-to-D Conversion Data Register								ADDATA
P073 to P07C	Reserved								
P07D	Port E Data Input Register								ADIN
P07E	Port E Input Enable Register								ADENA
P07F	**AD STEST**	**AD PRIORITY**	**AD ESPEN**	—	—	—	—	—	ADPRI

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC1}‡, V_{CC2}, V_{CC3} (see Note 2) . . . . . –0.6 V to 7 V
Input voltage range, All pins except MC . . . . . –0.6 V to 7 V
MC . . . . . –0.6 V to 14 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC1}$) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC1}$) . . . . . ±20 mA
Continuous output current per buffer, I_O ($V_O = 0$ to V_{CC1})§ . . . . . ±10 mA
Maximum I_{CC} current . . . . . 170 mA
Maximum I_{SS} current . . . . . – 170 mA
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range, T_A: L version . . . . . 0°C to 70°C
A version . . . . . – 40°C to 85°C
T version . . . . . – 40°C to 105°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ $V_{CC1} = V_{CC}$
§ Electrical characteristics are specified with all output buffers loaded with specified I_O current. Exceeding the specified I_O current in any buffer can affect the levels on other buffers.
NOTE 2: Unless otherwise noted, all voltage values are with respect to V_{SS1}.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage (see Note 2)		4.5	5	5.5	V
	RAM data-retention supply voltage (see Note 3)		3		5.5	
V_{CC2}	Digital I/O supply voltage (see Note 2)		4.5	5	5.5	V
V_{CC3}	Analog supply voltage (see Note 2)		4.5	5	5.5	
V_{SS2}	Digital I/O supply ground		– 0.3	0	0.3	V
V_{SS3}	Analog supply ground		– 0.3	0	0.3	V
V_{IL}	Low-level input voltage	All pins except MC	V_{SS1}		0.8	V
		MC, normal operation	V_{SS1}		0.3	V
V_{IH}	High-level input voltage	All pins except MC, XTAL2/CLKIN, and $\overline{\text{RESET}}$	2		V_{CC1}	V
		MC (non-WPO mode)	$V_{CC1}-0.3$		$V_{CC1}+0.3$	
		XTAL2/CLKIN	0.8 V_{CC1}		V_{CC1}	
		$\overline{\text{RESET}}$	0.7 V_{CC1}		V_{CC1}	
V_{MC}	MC (mode control) voltage (see Note 4)	EEPROM write protect override (WPO)	11.7	12	13	V
		EPROM programming voltage (V_{PP})	13	13.2	13.5	
		Microprocessor	$V_{CC1}-0.3$		$V_{CC1}+0.3$	
		Microcomputer	V_{SS1}		0.3	
T_A	Operating free-air temperature	L version	0		70	°C
		A version	– 40		85	
		T version	– 40		105	

NOTES: 2. Unless otherwise noted, all voltage values are with respect to V_{SS1}.
3. $\overline{\text{RESET}}$ must be externally activated when V_{CC1} or SYSCLK is not within the recommended operating range.
4. The basic microcomputer and microprocessor operating modes are selected by the voltage level applied to the dedicated MC pin two system-clock cycles (t_c) before $\overline{\text{RESET}}$ goes inactive (high). The WPO mode can be selected anytime a sufficient voltage is present on MC.

electrical characteristics over recommended operating free-air temperature range (unless

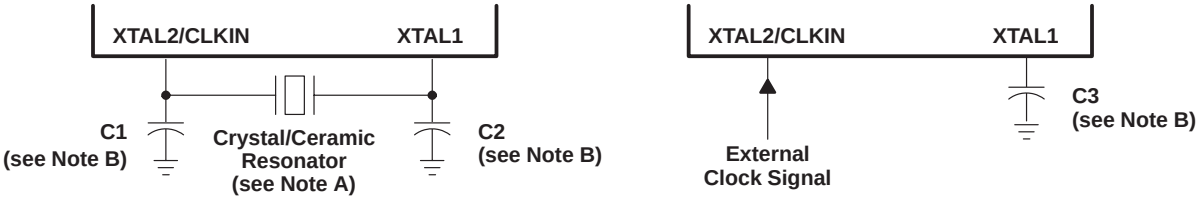
otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage (see Note 5)		I_{OL} = 1.4 mA				0.4	V
V_{OH}	High-level output voltage		I_{OH} = –50 µA		0.9 V_{CC1}			V
			I_{OH} = –2 mA		2.4			
I_I	Input current	MC	0 V < V_I ≤ 0.3 V				10	µA
			0.3 V < V_I < V_{CC1}–0.3 V				50	
			V_{CC1}–0.3 V ≤ V_I ≤ V_{CC1}+0.3 V				10	
			V_{CC1} + 0.3 V < V_I ≤ 13 V				650	
			12 V ≤ V_I ≤ 13 V	See Note 6			50	mA
		I/O pins	0 V ≤ V_I ≤ V_{CC1}				± 10	µA
I_{OL}	Low-level output current (see Note 5)		V_{OL} = 0.4 V		1.4			mA
I_{OH}	High-level output current		V_{OH} = 0.9 V_{CC1}		– 50			µA
			V_{OH} = 2.4 V		– 2			mA
I_{CC}	Supply current (operating mode) OSC POWER bit = 0 (see Note 9)	TMS370Cx50A TMS370Cx52A	SYSCLK = 5 MHz	See Notes 7 and 8		30	45	mA
		TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B				35	56	
		TMS370Cx50A TMS370Cx52A	SYSCLK = 3 MHz	See Notes 7 and 8		20	30	
		TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B				25	36	
		TMS370Cx59A†				46	55	
	Supply current (operating mode) OSC POWER bit = 0 (see Note 9)	TMS370Cx50A TMS370Cx52A	SYSCLK = 0.5 MHz	See Notes 7 and 8		5	11	mA
		TMS370Cx53A TMS370Cx56A TMS370Cx58A TMS370Cx58B				13	18	
		TMS370Cx59A†				22	28	
	Supply current (STANDBY mode) OSC POWER bit = 0 (see Note 10)		SYSCLK = 5 MHz,	See Notes 7 and 8		12	17	mA
			SYSCLK = 3 MHz,	See Notes 7 and 8		8	11	
			SYSCLK = 0.5 MHz,	See Notes 7 and 8		2.5	3.5	
	Supply current (STANDBY mode) OSC POWER bit = 1 (see Note 11)		SYSCLK = 3 MHz,	See Notes 7 and 8		6	8.6	mA
			SYSCLK = 0.5 MHz,	See Notes 7 and 8		2	3	
	Supply current (HALT mode)		XTAL2/CLKIN < 0.2 V,	See Note 7		2	30	µA

† TMS370Cx59 only operate up to 3 MHz SYSCLK

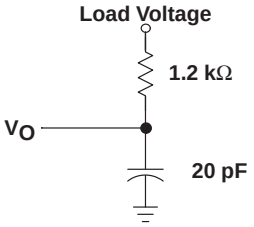
NOTES:
5. In prior versions of the TMS370 family, the I_{OL} current was equal to 2 mA for ports A, B, C, and D and the $\overline{RESET}$ pin.
6. Input current I_{PP} is a maximum of 50 mA only when the EPROM is being programmed.
7. Single chip mode, ports configured as inputs or outputs with no load. All inputs ≤ 0.2 V or ≥ V_{CC} – 0.2V.
8. XTAL2/CLKIN is driven with an external square wave signal with 50% duty cycle and rise and fall times less than 10 ns. Current can be higher with a crystal oscillator. At 5 MHz SYSCLK, this extra current = 0.01 mA x (total load capacitance + crystal capacitance in pF).
9. Maximum operating current for TMS370Cx50A and TMS370Cx52A = 7.6 (SYSCLK) + 7 mA. Maximum operating current for TMS370Cx53A, TMS370Cx56A, TMS370Cx58A, and TMS370Cx58B = 10 (SYSCLK) + 5.8 mA.
10. Maximum standby current for TMS370Cx5xA = 3 (SYSCLK) + 2 mA. (OSC POWER bit = 0).
11. Maximum standby current for TMS370Cx5xA and TMS370Cx5xB = 2.24 (SYSCLK) + 1.9 mA. (OSC POWER bit = 1, valid only up to 3 MHz of SYSCLK.)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The crystal/ceramic resonator frequency is four times the reciprocal of the system clock period.
B. The values of C1 and C2 are typically 15 pF and C3 is typically 50 pF. See the manufacturer's recommendations for ceramic resonators.

Figure 19. Recommended Crystal/Clock Connections



Case 1: $V_O = V_{OH}$ = 2.4 V; Load Voltage = 0 V
Case 2: $V_O = V_{OL}$ = 0.4 V; Load Voltage = 2.1 V

NOTE A: All measurements are made with the pin loading as shown unless otherwise noted. All measurements are made with XTAL2/CLKIN driven by an external square wave signal with a 50% duty cycle and rise and fall times less than 10 ns unless otherwise stated.

Figure 20. Typical Output Load Circuit (see Note A)

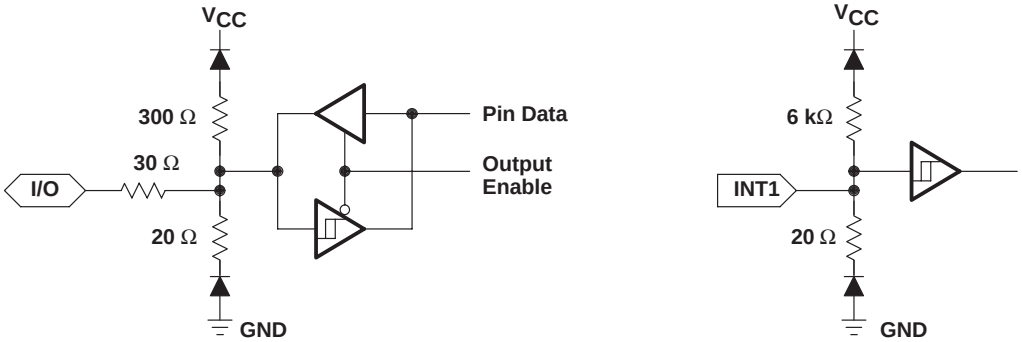


Figure 21. Typlcal Buffer Circuitry

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols have been created in accordance with JEDEC Standard 100. In order to shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

A	Address	RXD	SCIRXD
AR	Array	S	Slave mode
B	Byte	SC	SYSCLK
CI	XTAL2/CLKIN	SCC	SCICLK
D	Data	SIMO	SPISIMO
E	$\overline{\text{EDS}}$	SOMI	SPISOMI
FE	Final	SPC	SPICLK
IE	Initial	TXD	SCITXD
M	Master mode	W	Write
PGM	Program	WT	$\overline{\text{WAIT}}$
R	Read		

Lowercase subscripts and their meanings are:

c	cycle time (period)	r	rise time
d	delay time	su	setup time
f	fall time	v	valid time
h	hold time	w	pulse duration (width)

The following additional letters are defined as follows:

H	High
L	Low
V	Valid
Z	High impedance

All timings are measured between high and low measurement points as indicated in Figure 22 and Figure 23.

Figure 22. XTAL2/CLKIN Measurement Points

Figure 23. General Measurement Points

external clocking requirements for clock divided by 4†

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 12)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCL)}$	Delay time, XTAL2/CLKIN rise to SYSCLK fall		100	ns
	CLKIN‡	Crystal operating frequency	2	20	MHz
	SYSCLK§	System clock¶	0.5	5	MHz

† For V_{IL} and V_{IH}, refer to recommended operating conditions.
‡ 'x59A operates up to 12 MHz CLKIN
§ 'x59A operates up to 3 MHz SYSCLK
¶ SYSCLK = CLKIN/4
NOTE 12: This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

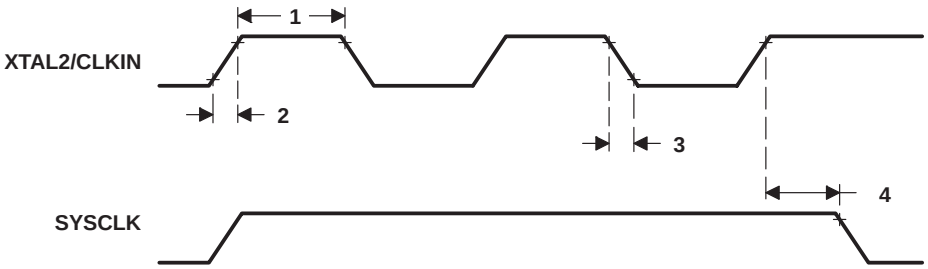


Figure 24. External Clock Timing for Divide-by-4

external clocking requirements for clock divided by 1 (PLL)†

NO.	PARAMETER		MIN	MAX	UNIT
1	$t_{w(Cl)}$	Pulse duration, XTAL2/CLKIN (see Note 12)	20		ns
2	$t_{r(Cl)}$	Rise time, XTAL2/CLKIN		30	ns
3	$t_{f(Cl)}$	Fall time, XTAL2/CLKIN		30	ns
4	$t_{d(CIH-SCH)}$	Delay time, XTAL2/CLKIN rise to SYSCLK rise		100	ns
	CLKIN#	Crystal operating frequency	2	5	MHz
	SYSCLK§	System clock‖	2	5	MHz

† For V_{IL} and V_{IH}, refer to recommended operating conditions.
§ 'x59A operates up to 3 MHz SYSCLK
# 'x59A operates up to 3 MHz CLKIN (for divide-by-1 clock option)
‖ SYSCLK = CLKIN/1
NOTE 12: This pulse can be either a high pulse which extends from the earliest valid high to the final valid high in an XTAL2/CLKIN cycle, or a low pulse, which extends from the earliest valid low to the final valid low in an XTAL2/CLKIN cycle.

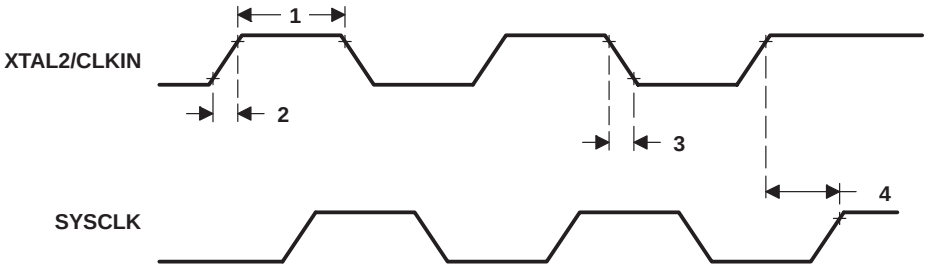


Figure 25. External Clock Timing for Divide-by-1

general purpose output signal-switching time requirements

		MIN	NOM	MAX	UNIT
t_r	Rise time		30		ns
t_f	Fall time		30		ns

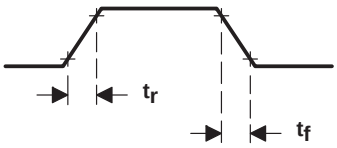


Figure 26. Signal-Switching Timing

recommended EEPROM timing requirements for programming

		MIN	MAX	UNIT
$t_{w(PGM)B}$	Pulse duration, programming signal to ensure valid data is stored (byte mode)	10		ms
$t_{w(PGM)AR}$	Pulse duration, programming signal to ensure valid data is stored (array mode)	20		ms

recommended EPROM operating conditions for programming

			MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage		4.75	5.5	6	V
V_{PP}	Supply voltage at MC pin		13	13.2	13.5	V
I_{PP}	Supply current at MC pin during programming (V_{PP} = 13 V)			30	50	mA
SYSCLK	System clock	Divide-by-4	0.5		5	MHz
		Divide-by-1	2		5	

recommended EPROM timing requirements for programming

		MIN	NOM	MAX	UNIT
$t_{w(EPGM)}$	Pulse duration, programming signal (see Note 13)	0.40	0.50	3	ms

NOTE 13: Programming pulse is active when both EXE (EPCTL.0) and V_{PPS} (EPCTL.6) are set.

switching characteristics and timing requirements for external read and write (see Figure 27 and Figure 28)†

NO.	PARAMETER			MIN	MAX	UNIT
5	t_c	Cycle time, SYSCLK (system clock)	Divide-by-4 clock	200	2000	ns
			Divide-by-1 PLL	200	500	
6	$t_{w(SCL)}$	Pulse duration, SYSCLK low		$0.5t_c$–25	$0.5t_c$	ns
7	$t_{w(SCH)}$	Pulse duration, SYSCLK high		$0.5t_c$	$0.5t_c$+20	ns
8	$t_{d(SCL-A)}$	Delay time, SYSCLK low to address R/$\overline{W}$ and $\overline{OCF}$ valid			$0.25t_c$+75	ns
9	$t_{v(A)}$	Valid time, address to $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low		$0.5t_c$–90		ns
10	$t_{su(D)}$	Setup time, write data time to $\overline{EDS}$ high		$0.75t_c$–80‡		ns
11	$t_{h(EH-A)}$	Hold time, address, R/$\overline{W}$ and $\overline{OCF}$ from $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ high		$0.5t_c$–60		ns
12	$t_{h(EH-D)W}$	Hold time, write data time from $\overline{EDS}$ high		$0.75t_c$+15		ns
13	$t_{d(DZ-EL)}$	Delay time, data bus high impedance to $\overline{EDS}$ low (read cycle)		$0.25t_c$–35		ns
14	$t_{d(EH-D)}$	Delay time, $\overline{EDS}$ high to data bus enable (read cycle)		$1.25t_c$–40		ns
15	$t_{d(EL-DV)R}$	Delay time, $\overline{EDS}$ low to read data valid			t_c–95‡	ns
16	$t_{h(EH-D)R}$	Hold time, read time from $\overline{EDS}$ high		0		ns
17	$t_{su(WT-SCH)}$	Setup time, $\overline{WAIT}$ time to SYSCLK high		$0.25t_c$+70§		ns
18	$t_{h(SCH-WT)}$	Hold time, $\overline{WAIT}$ time from SYSCLK high		0		ns
19	$t_{d(EL-WTV)}$	Delay time, $\overline{EDS}$ low to $\overline{WAIT}$ valid			$0.5t_c$–60	ns
20	t_w	Pulse duration, $\overline{EDS}$, $\overline{CSE1}$, $\overline{CSE2}$, $\overline{CSH1}$, $\overline{CSH2}$, $\overline{CSH3}$, and $\overline{CSPF}$ low		t_c–80‡	t_c+40‡	ns
21	$t_{d(AV-DV)R}$	Delay time, address valid to read data valid			$1.5t_c$–115‡	ns
22	$t_{d(AV-WTV)}$	Delay time, address valid to $\overline{WAIT}$ valid			t_c–115	ns
23	$t_{d(AV-EH)}$	Delay time, address valid to $\overline{EDS}$ high (end of write)		$1.5t_c$–85‡		ns

† t_c = system-clock cycle time = 1/SYSCLK
‡ If wait states, PFWait, or the autowait feature is used, add t_c to this value for each wait state invoked.
§ If the autowait feature is enabled, the $\overline{WAIT}$ input can assume a “don’t care” condition until the third cycle of the access. The $\overline{WAIT}$ signal must be synchronized with the high pulse of the SYSCLK signal while still conforming to the minimum setup time.

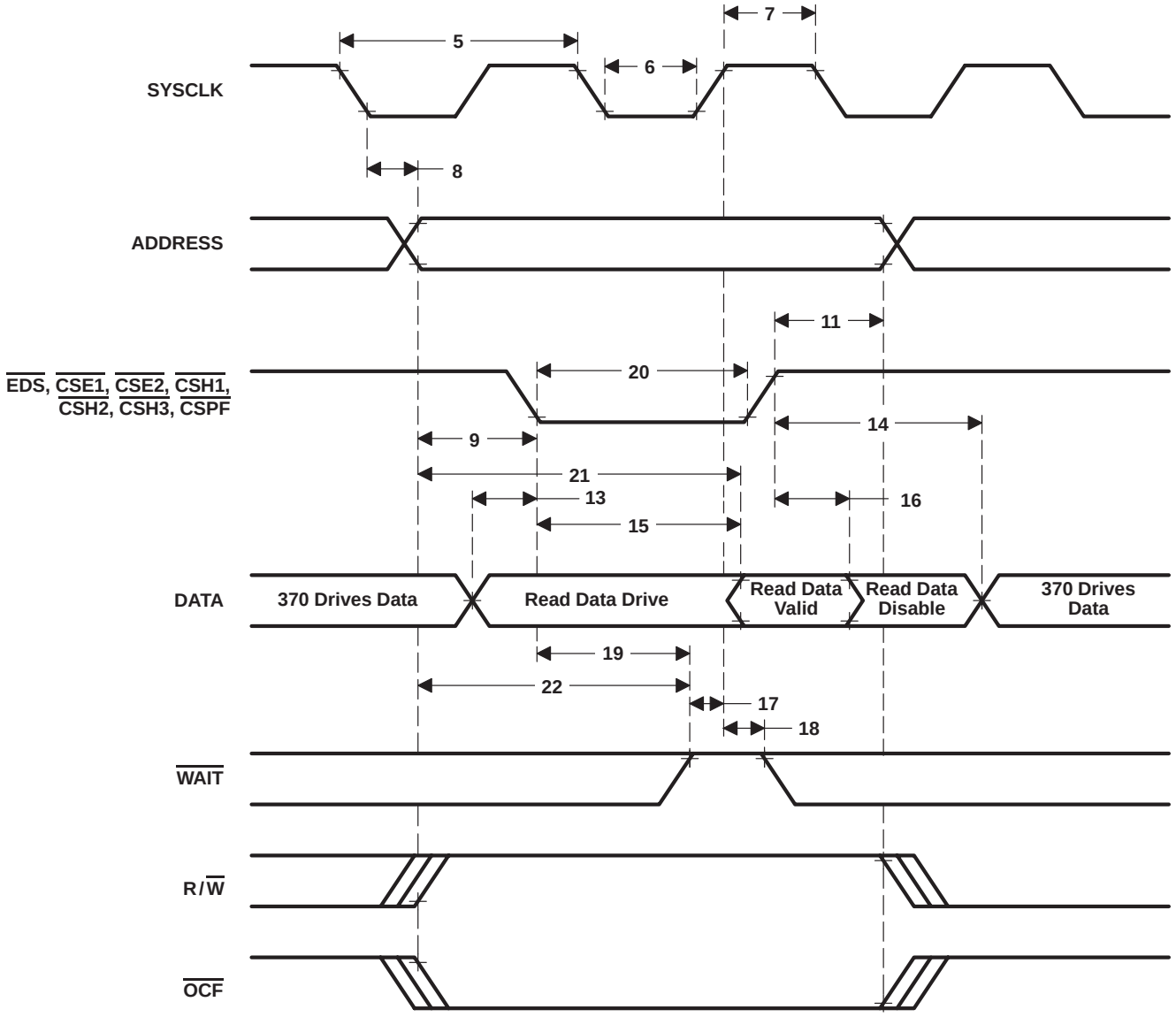


Figure 27. Switching Characteristics and Timing Requirements for External-Read

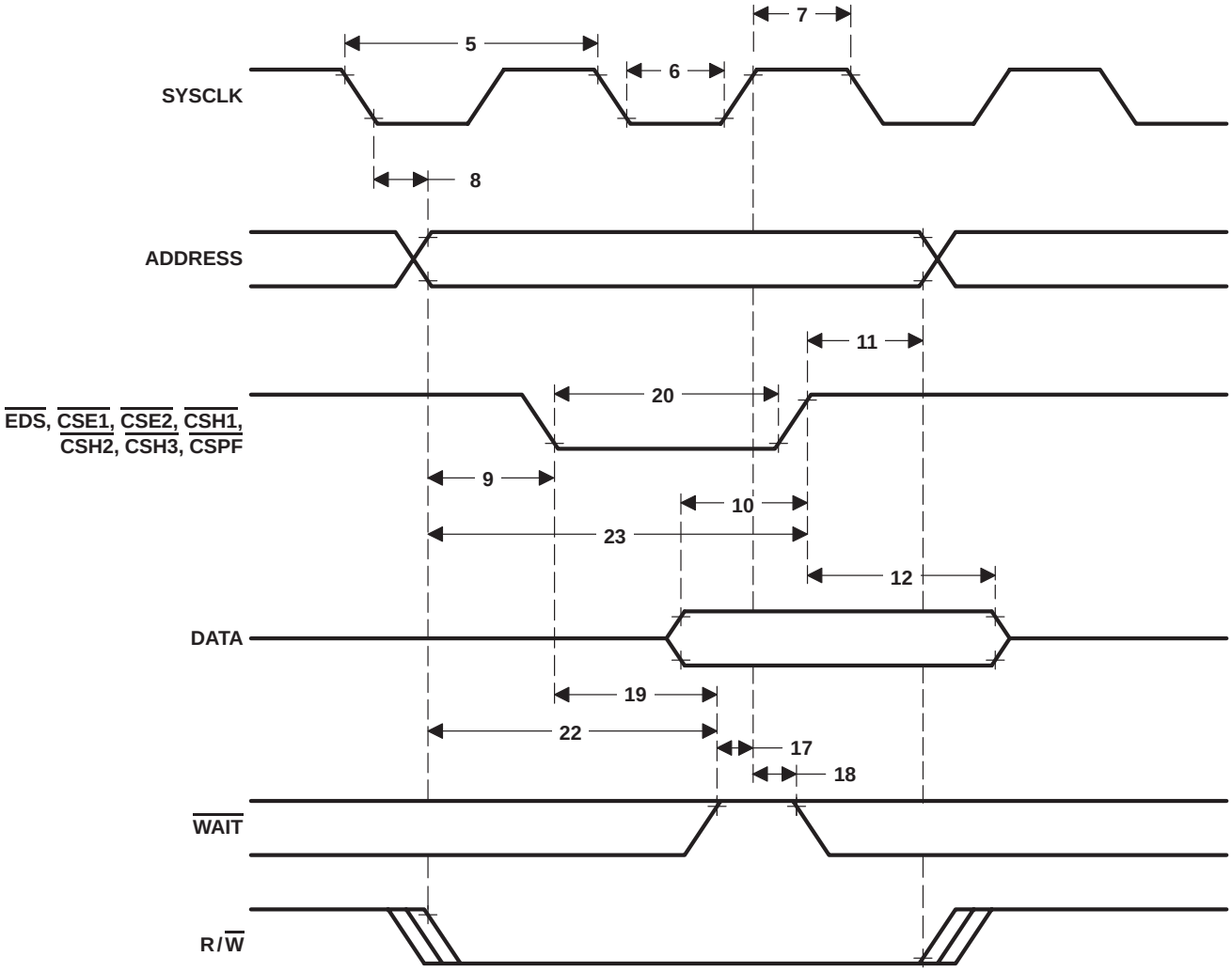


Figure 28. Switching Characteristics and Timing Requirements for External-Write

SCI1 isosynchronous† mode timing characteristics and requirements for internal clock (see Note 14 and Figure 29)

NO.			MIN	MAX	UNIT
24	$t_{c(SCC)}$	Cycle time, SCICLK	$2t_c$	$131072t_c$	ns
25	$t_{w(SCCL)}$	Pulse duration, SCICLK low	t_c – 45	$0.5t_{c(SCC)}$+45	ns
26	$t_{w(SCCH)}$	Pulse duration, SCICLK high	t_c – 45	$0.5t_{c(SCC)}$+45	ns
27	$t_{d(SCCL-TXDV)}$	Delay time, SCITXD valid after SCICLK low	– 50	60	ns
28	$t_{v(SCCH-TXD)}$	Valid time, SCITXD data valid after SCICLK high	$t_{w(SCCH)}$ – 50		ns
29	$t_{su(RXD-SCCH)}$	Setup time, SCIRXD to SCICLK high	0.25 t_c + 145		ns
30	$t_{v(SCCH-RXD)}$	Valid time, SCIRXD data valid after SCICLK high	0		ns

NOTE 14: t_c = system-clock cycle time = 1/SYSCLK

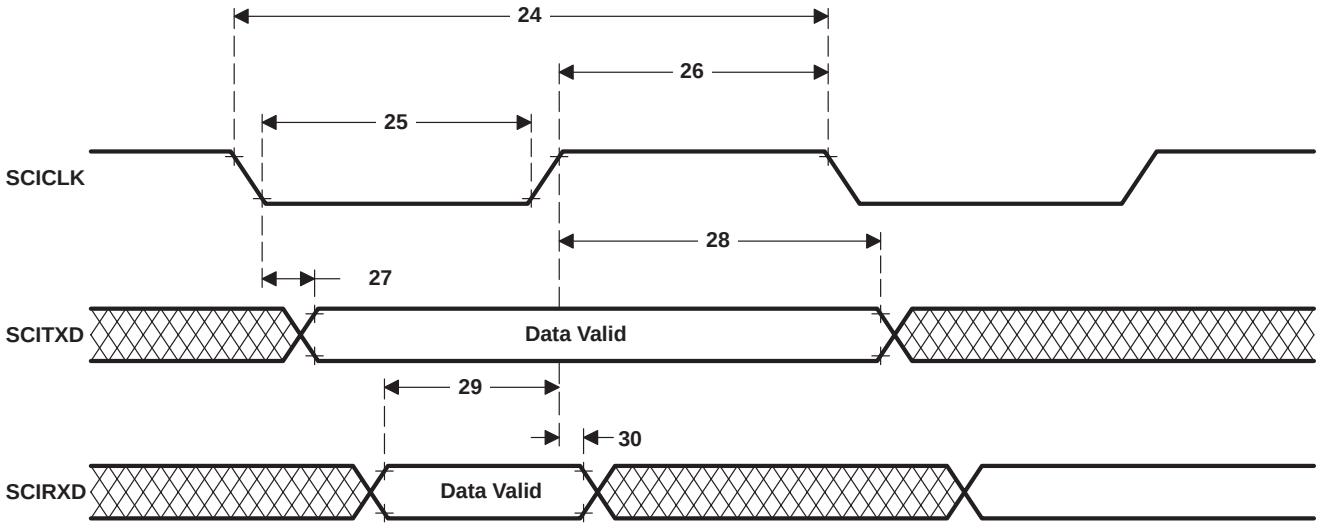


Figure 29. SCI1 Isosynchronous† Mode Timing for Internal Clock

† Isosynchronous = Isochronous

SCI1 isosynchronous† mode timing characteristics and requirements for external clock (see Note 14 and Figure 30)

NO.			MIN	MAX	UNIT
31	$t_{c(SCC)}$	Cycle time, SCICLK	$10t_c$		ns
32	$t_{w(SCCL)}$	Pulse duration, SCICLK low	$4.25t_c + 120$		ns
33	$t_{w(SCCH)}$	Pulse duration, SCICLK high	$t_c + 120$		ns
34	$t_{d(SCCL-TXDV)}$	Delay time, SCITXD valid after SCICLK low		$4.25t_c + 145$	ns
35	$t_{v(SCCH-TXD)}$	Valid time, SCITXD data valid after SCICLK high	$t_{w(SCCH)}$		ns
36	$t_{su(RXD-SCCH)}$	Setup time, SCIRXD to SCICLK high	40		ns
37	$t_{v(SCCH-RXD)}$	Valid time, SCIRXD data after SCICLK high	$2t_c$		ns

NOTE 14: t_c = system-clock cycle time = 1/SYSCLK

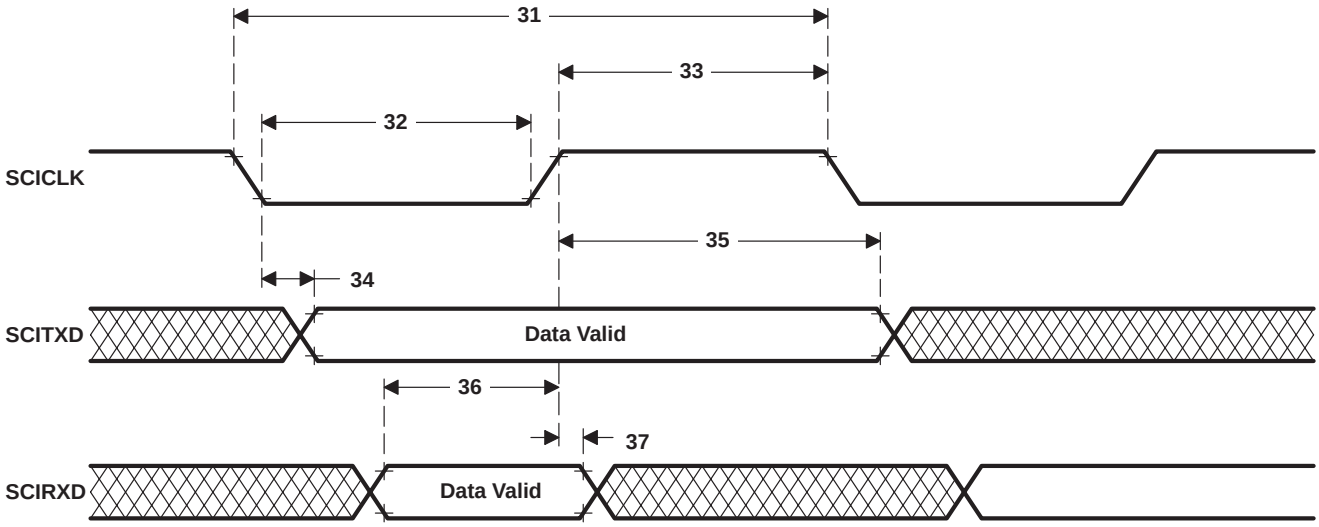


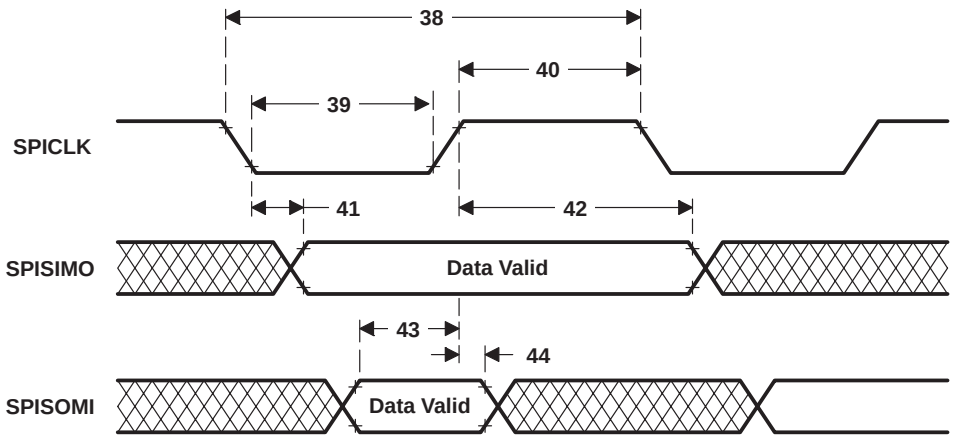
Figure 30. SCI1 Isosynchronous† Timing for External Clock

† Isosynchronous = Isochronous

SPI master mode external timing characteristics and requirements (see Note 14 and Figure 31)

NO.			MIN	MAX	UNIT
38	$t_{c(SPC)M}$	Cycle time, SPICLK	$2t_c$	$256t_c$	ns
39	$t_{w(SPCL)M}$	Pulse duration, SPICLK low	t_c – 45	$0.5t_{c(SPC)}$+45	ns
40	$t_{w(SPCH)M}$	Pulse duration, SPICLK high	t_c – 55	$0.5t_{c(SPC)}$+45	ns
41	$t_{d(SPCL-SIMOV)M}$	Delay time, SPISIMO valid after SPICLK low (polarity = 1)	– 65	50	ns
42	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (polarity =1)	$t_{w(SPCH)}$ – 50		ns
43	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI to SPICLK high (polarity = 1)	0.25 t_c + 150		ns
44	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (polarity = 1)	0		ns

NOTE 14: t_c = system-clock cycle time = 1/SYSCLK



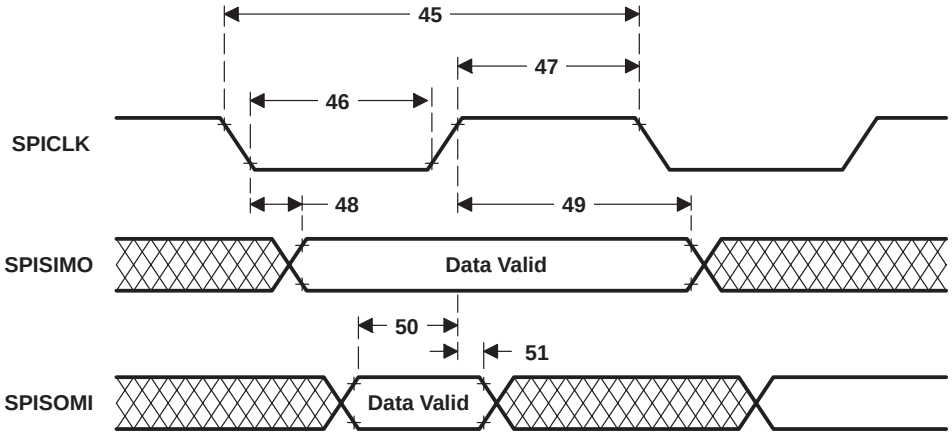
NOTE A: The diagram shows polarity = 1. SPICLK is inverted when polarity = 0.

Figure 31. SPI Master External Timing

SPI slave mode external timing characteristics and requirements (see Note 14 and Figure 32)

NO.			MIN	MAX	UNIT
45	$t_{c(SPC)S}$	Cycle time, SPICLK	$8t_c$		ns
46	$t_{w(SPCL)S}$	Pulse duration, SPICLK low	$4t_c$ – 45	$0.5t_{c(SPC)S}$+45	ns
47	$t_{w(SPCH)S}$	Pulse duration, SPICLK high	$4t_c$ – 45	$0.5t_{c(SPC)S}$+45	ns
48	$t_{d(SPCL-SOMIV)S}$	Delay time, SPISOMI valid after SPICLK low (polarity = 1)		$3.25t_c$ + 130	ns
49	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (polarity =1)	$t_{w(SPCH)S}$		ns
50	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO to SPICLK high (polarity = 1)	0		ns
51	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data after SPICLK high (polarity = 1)	$3t_c$ + 100		ns

NOTE 14: t_c = system-clock cycle time = 1/SYSCLK



NOTE A: The diagram shows polarity = 1. SPICLK is inverted when polarity = 0.

Figure 32. SPI-Slave External Timing

The ADC1 has a separate power bus for its analog circuitry. These pins are referred to as V_{CC3} and V_{SS3}. The purpose is to enhance ADC1 performance by preventing digital switching noise of the logic circuitry that can be present on V_{SS1} and V_{CC1} from coupling into the ADC1 analog stage. All ADC1 specifications are given with respect to V_{SS3} unless otherwise noted.

Resolution . . . . . 8-bits (256 values)
Monotonic . . . . . Yes
Output conversion mode . . . . . 00h to FFh (00 for VI ≤ V_{SS3} ≤; FF for VI ≤ V_{ref})
Conversion time (excluding sample time) . . . . . 164 t_c

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC3}	Analog supply voltage	4.5	5	5.5	V
		V_{CC1}–0.3		V_{CC1}+0.3	
V_{SS3}	Analog ground	V_{SS1}–0.3		V_{SS1}+0.3	V
V_{ref}	Non-V_{CC3} reference†	2.5	V_{CC3}	V_{CC3} + 0.1	V
	Analog input for conversion	V_{SS3}		V_{ref}	V

† V_{ref} must be stable, within ± 1/2 LSB of the required resolution, during the entire conversion time.

operating characteristics over recommended ranges operating conditions

PARAMETER			MIN	MAX	UNIT
	Absolute accuracy‡	V_{CC3} = 5.5 V V_{ref} = 5.1 V		±1.5	LSB
	Differential/integral linearity error‡§	V_{CC3} = 5.5 V V_{ref} = 5.1 V		±0.9	LSB
I_{CC3}	Analog supply current	Converting		2	mA
		Nonconverting		5	µA
I_I	Input current, AN0 – AN7	0 V ≤ V_I ≤ 5.5 V		2	µA
	I_{ref} input charge current			1	mA
Z_{ref}	Source impedance of V_{ref}	SYSCLK ≤ 3 MHz		24	kΩ
		3 MHz < SYSCLK ≤ 5 MHz		10	kΩ

‡ Absolute resolution = 20 mV. At V_{ref} = 5 V, this is one LSB. As V_{ref} decreases, LSB size decreases; therefore, the absolute accuracy and differential/integral linearity errors in terms of LSBs increase.
§ Excluding quantization error of 1/2 LSB

The ADC1 module allows complete freedom in design of the sources for the analog inputs. The period of the sample time is user-defined so that the high-impedance can be accommodated without penalty to the low-impedance sources. The sample period begins when the SAMPLE START bit of the ADC1 control register (ADCTL.6) is set to 1. The end of the signal sample period occurs when the conversion bit (CONVERT START, ADCTL.7) is set to 1. After a hold time, the converter will reset the SAMPLE START and CONVERT START bits, signaling that a conversion has started and that the analog signal can be removed.

analog timing requirements

		MIN	MAX	UNIT
$t_{su(S)}$	Setup time, analog to sample command	0		ns
$t_{h(AN)}$	Hold time, analog input from start of conversion	$18t_c$		ns
$t_{w(S)}$	Pulse duration, sample time per kilohm of source impedance†	1		µs/kΩ

† The value given is valid for a signal with a source impedance > 1 kΩ. If the source impedance is < 1 kΩ, use a minimum sampling time of 1µs.

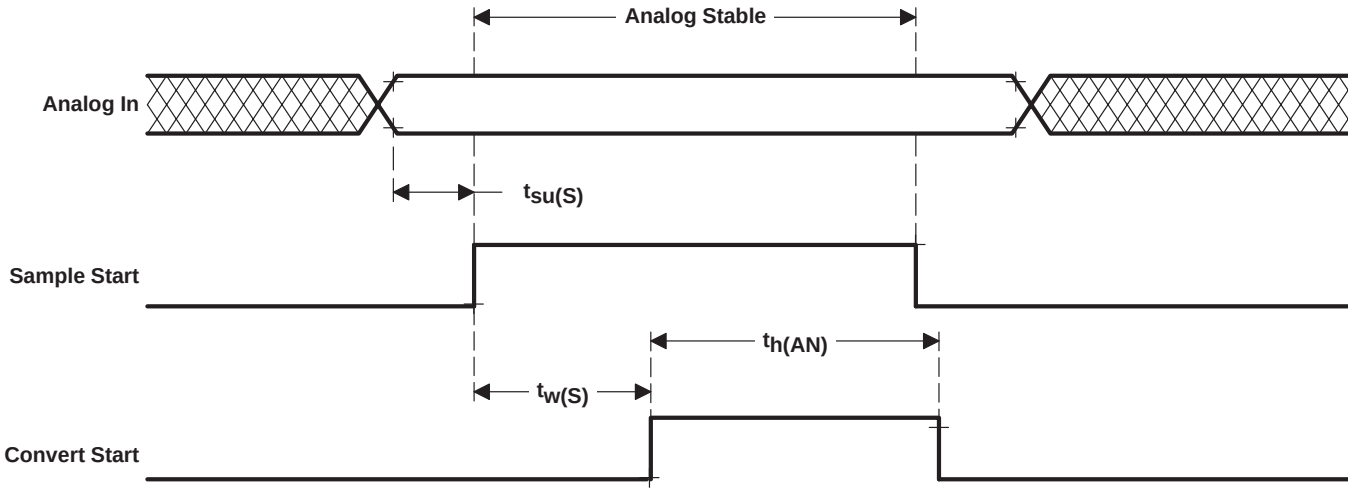


Figure 33. Analog Timing

Table 26 is designed to aid the user in referencing a device part number to a mechanical drawing. The table shows a cross-reference of the device part number to the TMS370 generic package name and the associated mechanical drawing by drawing number and name.

Table 26. TMS370Cx5x Family Package Type and Mechanical Cross-Reference

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
FN – 68 pin (50-mil pin spacing)	PLASTIC LEADED CHIP CARRIER (PLCC)	FN(S-PQCC-J**) PLASTIC J-LEADED CHIP CARRIER	TMS370C050AFNA TMS370C050AFNL TMS370C050AFNT TMS370C150AFNT TMS370C250AFNT TMS370C350AFNA TMS370C350AFNL TMS370C350AFNT TMS370C052AFNA TMS370C052AFNL TMS370C052AFNT TMS370C352AFNA TMS370C352AFNL TMS370C352AFNT TMS370C452AFNA TMS370C452AFNL TMS370C452AFNT TMS370C353AFNA TMS370C353AFNL TMS370C353AFNT TMS370C056AFNA TMS370C056AFNL TMS370C056AFNT TMS370C156AFNT TMS370C256AFNT TMS370C356AFNA TMS370C356AFNL TMS370C356AFNT TMS370C456AFNA TMS370C456AFNL TMS370C456AFNT TMS370C756AFNT TMS370C058AFNA TMS370C058AFNL TMS370C058AFNT TMS370C358AFNA TMS370C358AFNL TMS370C358AFNT TMS370C758AFNT TMS370C758BFNT TMS370C059AFNA TMS370C059AFNL TMS370C059AFNT TMS370C759AFNT
FZ – 68 pin (50-mil pin spacing)	CERAMIC LEADED CHIP CARRIER (CLCC)	FZ(S-CQCC-J**) J-LEADED CERAMIC CHIP CARRIER	SE370C756AFZT SE370C758AFZT SE370C758BFZT SE370C759AFZT
JN – 64 pin (70-mil pin spacing)	CERAMIC SHRINK DUAL-IN-LINE PACKAGE (CSDIP)	JN(R-CDIP-T64) CERAMIC DUAL-IN-LINE PACKAGE	SE370C756AJNT SE370C758AJNT SE370C758BJNT

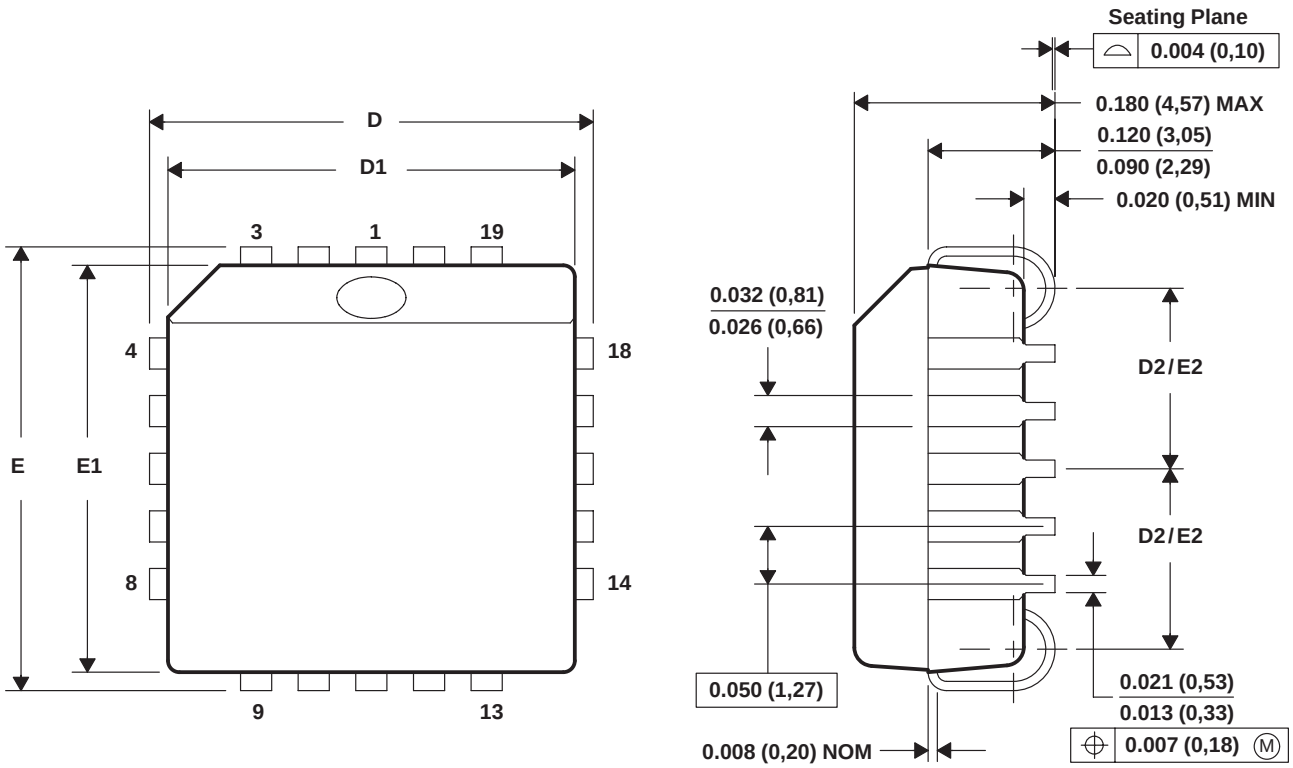
Table 26. TMS370Cx5x Family Package Type and Mechanical Cross-Reference (Continued)

PKG TYPE (mil pin spacing)	TMS370 GENERIC NAME	PKG TYPE NO. AND MECHANICAL NAME	DEVICE PART NUMBERS
NM – 64 pin (70-mil pin spacing)	PLASTIC SHRINK DUAL-IN-LINE PACKAGE (PSDIP)	NM(R-PDIP-T64) PLASTIC SHRINK DUAL-IN-LINE PACKAGE	TMS370C050ANMA TMS370C050ANML TMS370C050ANMT TMS370C350ANMA TMS370C350ANML TMS370C350ANMT TMS370C052ANMA TMS370C052ANML TMS370C052ANMT TMS370C352ANMA TMS370C352ANML TMS370C352ANMT TMS370C056ANMA TMS370C056ANML TMS370C056ANMT TMS370C356ANMA TMS370C356ANML TMS370C356ANMT TMS370C756ANMT TMS370C058ANMA TMS370C058ANML TMS370C058ANMT TMS370C358ANMA TMS370C358ANML TMS370C358ANMT TMS370C758ANMT TMS370C758BNMT

MECHANICAL DATA

FN (S-PQCC-J)** **PLASTIC J-LEADED CHIP CARRIER**

20 PIN SHOWN



NO. OF PINS **	D / E		D1 / E1		D2 / E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

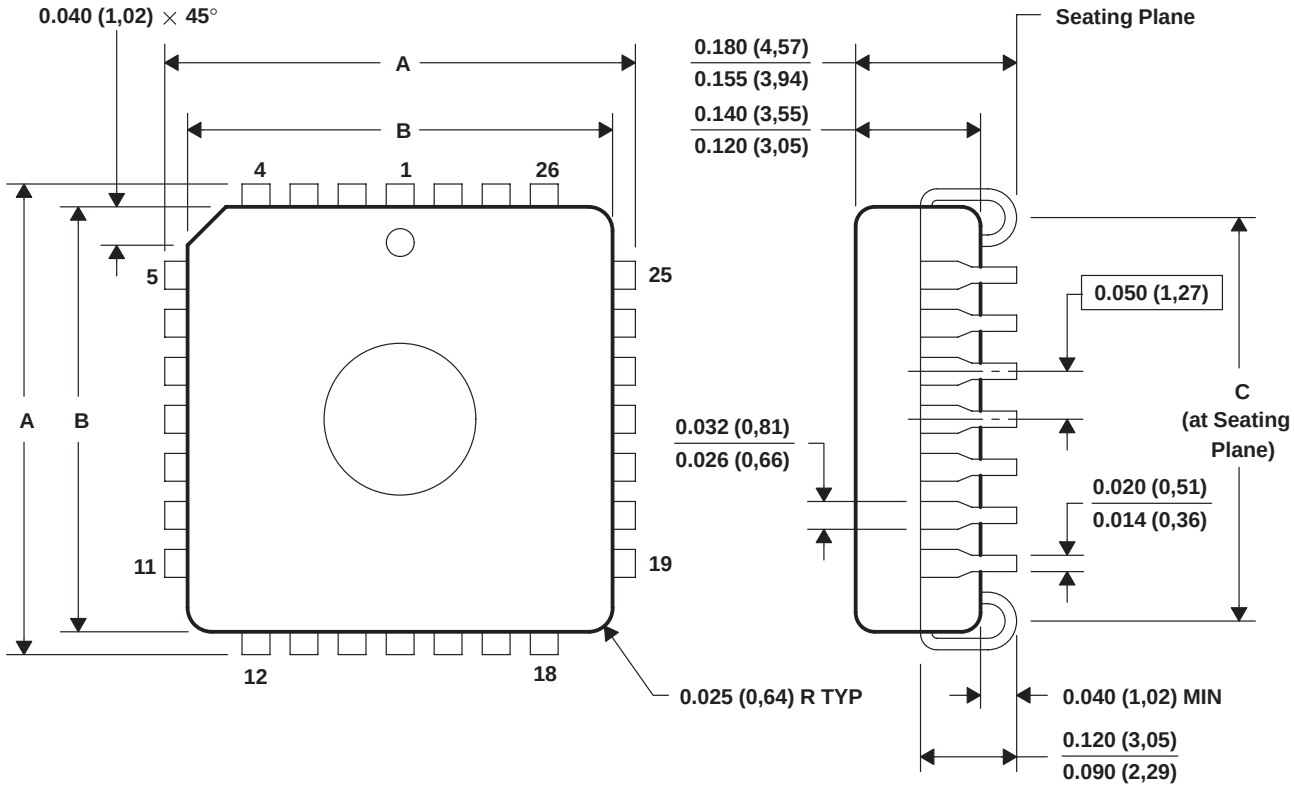
4040005 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

MECHANICAL DATA

FZ (S-CQCC-J)** **J-LEADED CERAMIC CHIP CARRIER**

28 LEAD SHOWN



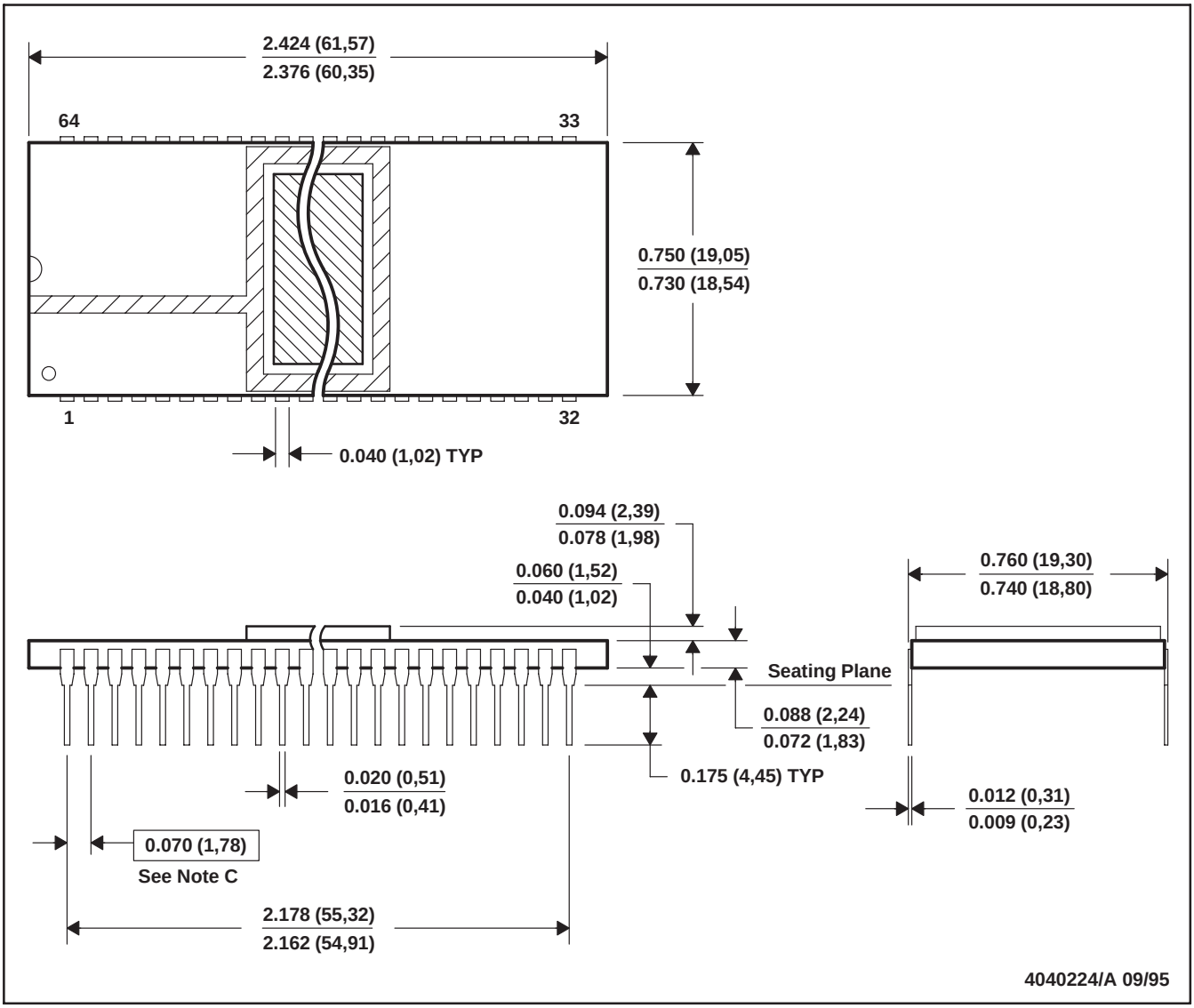
JEDEC OUTLINE	NO. OF PINS**	A		B		C	
		MIN	MAX	MIN	MAX	MIN	MAX
MO-087AA	28	0.485 (12,32)	0.495 (12,57)	0.430 (10,92)	0.455 (11,56)	0.410 (10,41)	0.430 (10,92)
MO-087AB	44	0.685 (17,40)	0.695 (17,65)	0.630 (16,00)	0.655 (16,64)	0.610 (15,49)	0.630 (16,00)
MO-087AC	52	0.785 (19,94)	0.795 (20,19)	0.730 (18,54)	0.765 (19,43)	0.680 (17,28)	0.740 (18,79)
MO-087AD	68	0.985 (25,02)	0.995 (25,27)	0.930 (23,62)	0.955 (24,26)	0.910 (23,11)	0.930 (23,62)

4040219 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.

MECHANICAL DATA

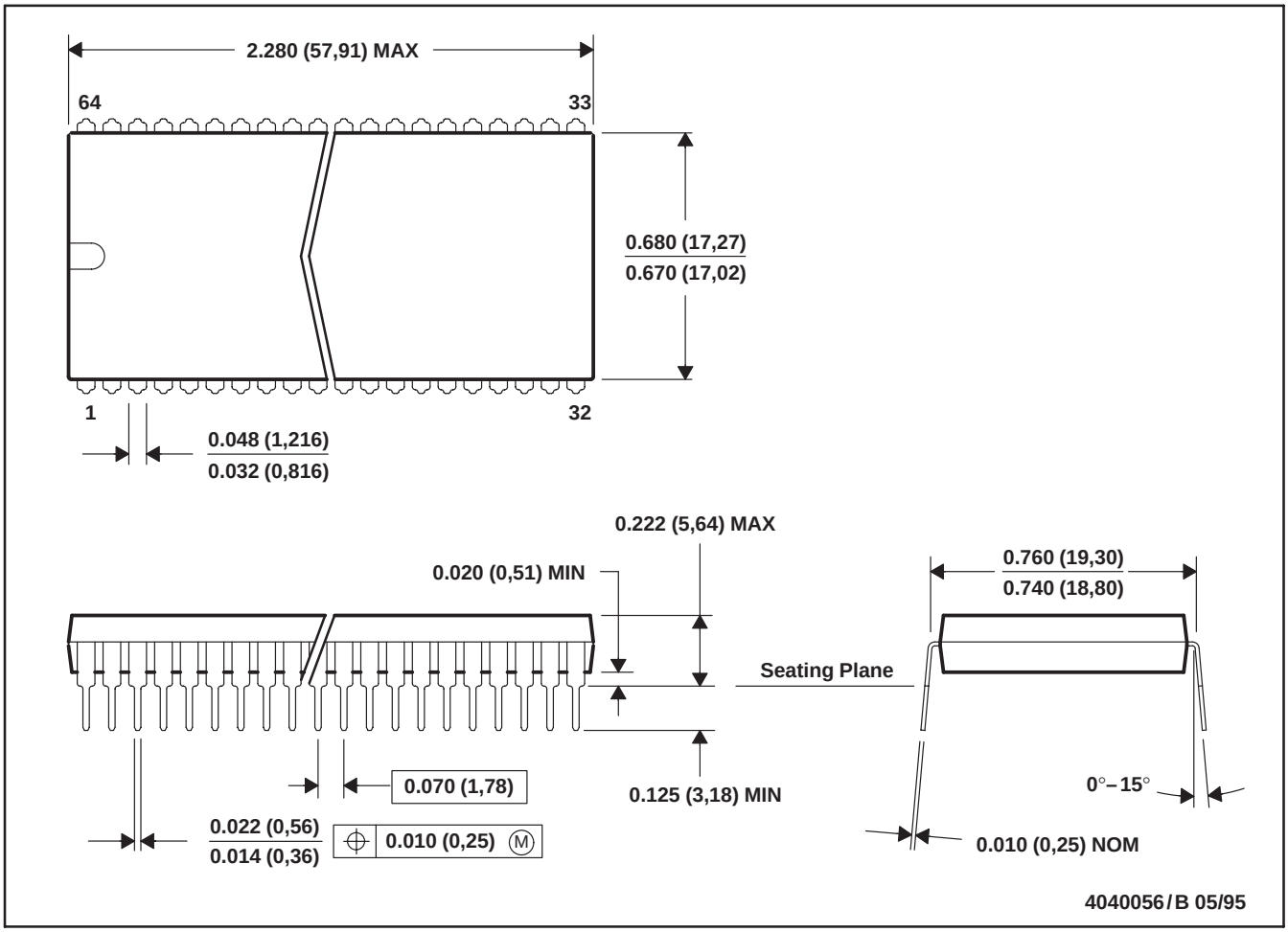
JN (R-CDIP-T64) **CERAMIC DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Each pin centerline located within 0.010 (0,26) of it true longitudinal position.

MECHANICAL DATA

NM (R-PDIP-T64) **PLASTIC SHRINK DUAL-IN-LINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

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